February 21, 2003

File 344:Chinese Patents Abs Aug 1985-2003/Jan
(c) 2003 European Patent Office
File 347:JAPIO Oct 1976-2002/Oct(Updated 030204)
(c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200312
(c) 2003 Thomson Derwent

Set	Items	Description
S1	348	SUBSCRIBER?()LINE?()INTERFACE?()CIRCUIT?
S2	382781	INTEGRATED()CIRCUIT? OR IC OR (PC OR PCMCIA OR MEMORY OR ROM OR RAM OR CHIP OR PLUGIN)(2N)CARD? OR INSERTION()BOARD? OR ASIC OR DISCRETE()COMPONENT?
S3	929982	SEMICONDUCTOR? OR CMOS OR NMOS OR PMOS OR (COMPLEMENTARY OR POSITIVE()CHANNEL OR NEGATIVE()CHANNEL)()METAL()OXIDE()SEMICONDUCTOR?
S4	2064758	TIP OR SEND? OR DISPATCH? OR TRANSMIT? OR TRANSMISS?
S5	2375912	RING OR RETURN? OR RECEIV?
S6	3009642	SENSE? OR SENSOR? OR SENSING OR DETECT? OR RECOGNI? OR ISOLAT? OR CALCULAT? OR IDENTIF? OR UNCOVER? OR DIAGNOS?
S7	2040833	ADJUST? OR ACCLIMAT? OR ACCOMODAT? OR ADAPT? OR CONFORM? OR TAILOR? OR MODIF? OR ALTER? OR CUSTOMI? OR READJUST?
S8	5088192	CURRENT? OR VOLT? OR POWER? OR ELECTRIC? OR SIGNAL?
S9	3337	LINEFEED? OR LINE()FEED?
S10	5	S1 AND S2 AND S3
S11	29	S1 AND (S2 OR S3)
S12	11	S11 AND S4 AND S5
S13	10	S12 NOT S10
S14	637429	S6(3N)S8
S15	149474	S7(3N)S8
S16	87	S1 AND (S14 OR S15)
S17	2	S16 AND S9
S18	2	S17 NOT (S13 NOT S10)
S19	32	S16 AND S4 AND S5
S20	29	S19 NOT (S18 OR S13 OR S10)
S21	0	S20 AND (S2 OR S3)
S22	1481	S2 AND S3 AND S4 AND S5
S23	187	S22 AND (S14 OR S15)
S24	0	S23 AND S9
S25	2	S23 AND IC=(H04M-003/00 OR H04M-019/00)
S26	2	S25 NOT (S20 OR S18 OR S10)
S27	120714	S2 AND S3
S28	220492	S4(5N)S5
S29	532	S27 AND S28
S30	51	S29 AND (S14 OR S15)
S31	49	S30 NOT (S26 OR S20 OR S18 OR S10)
S32	0	S31 AND S9
S33	22	S29(10N)(S14 OR S15)
S34	20	S33 NOT (S26 OR S20 OR S18 OR S10)

13/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014912798
WPI Acc No: 2002-733504/200280
XRPX Acc No: N02-578317
Subscriber line interface circuit **and its polarity reversing method**
Patent Assignee: HUAWEI TECHN CO LTD (HUAW-N)
Inventor: LIN W; SUN H; WANG B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CN 1358013	A	20020710	CN 2000136230	A	20001214	200280	B

Priority Applications (No Type Date): CN 2000136230 A 20001214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CN 1358013	A			H04M-001/738	

Abstract (Basic): CN 1358013 A
NOVELTY - An user's line interface circuit which can realize polarity reverse simply and suitable in use for **IC** is disclosed in which the RENG driver is connected to a form of reverse phase amplifier to make reverse phase amplifying of AC-DC signal exported by **TIP** driver for establishing the correlation between the output potentials of **TIP** driver and **RING** driver to realize the polarity reverse by adjusting the output **IC** potential of **TIP** driver.
DwgNo 0/0
Title Terms: SUBSCRIBER; LINE; INTERFACE; CIRCUIT; POLARITY; REVERSE; METHOD
Derwent Class: W01
International Patent Class (Main): H04M-001/738
File Segment: EPI

13/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014903808
WPI Acc No: 2002-724514/200279
XRPX Acc No: N02-571276
Subscriber line interface circuit **and its polarity reversing method**
Patent Assignee: HUAWEI TECHN CO LTD (HUAW-N)
Inventor: LIN W; SUN H; WANG B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CN 1358012	A	20020710	CN 2000136228	A	20001214	200279	B

Priority Applications (No Type Date): CN 2000136228 A 20001214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CN 1358012	A			H04M-001/738	

Abstract (Basic): CN 1358012 A
NOVELTY - An user's line interface circuit that can realized polarity reverse simply and suitable in use of **IC** is disclosed, in which the **RING** driver is connected to a form of reverse phase amplifier to make reverse phase amplifying for AC-DC signal exported by **TIP** driver, so that the correlation between the output potentials of **TIP** driver and **RING** driver is established. The output DC potential

of TID driver can be adjusted easily to realize the polarity reverse function in telephone loop by adopting branch voltage and electronic switch connected in series between DC power source to produce the different DC ouptut potential through controlling the electronic switch flow.

DwgNo 0/0

Title Terms: SUBSCRIBER; LINE; INTERFACE; CIRCUIT; POLARITY; REVERSE; METHOD

Derwent Class: W01

International Patent Class (Main): H04M-001/738

File Segment: EPI

13/5/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014859193 **Image available**

WPI Acc No: 2002-679899/200273

Subscriber interface circuit in full electronic switching system

Patent Assignee: YEON WOO ELECTRONICS & TELECOM CO LTD (YEON-N)

Inventor: KANG J Y; YOON D M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002035660	A	20020515	KR 200065739	A	20001107	200273	B

Priority Applications (No Type Date): KR 200065739 A 20001107

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002035660	A		1	H04M-003/30	

Abstract (Basic): KR 2002035660 A

NOVELTY - A subscriber interface circuit in a full electronic switching system is provided to accept all the merits of a transformer and an SLIC(**Subscriber Line Interface Circuit**) **IC** (**Integrated Circuit**) and to hybridize individual parts having high **transmission** characteristics.

DETAILED DESCRIPTION - Transistors(Q3,Q31)(Q2,Q21) supply call current to a subscriber through a **tip** terminal and a **ring** terminal, and amplify voice signal power. Transistors(Q1,Q11) limit the maximum call current. A transistor(Q4) detects call current, limits the base current of the transistor(Q11), and controls the maximum call current. A resistor(R12) connects between the transistors(Q3,Q31)(Q2,Q21), detects call current, converts it into voltage, and provides it between the base and emitter of the transistor(Q4). A transistor(Q5) controls the potential of the resistor(R12) through the transistors(Q1,Q11) and adjusts the limit range of the maximum call current. A transistor(Q7) adjusts the base potential of the transistor(Q11) according to a power-off control signal and controls the operation mode and interruption mode of the transistors(Q3,Q31). An operation amplifier(U1A) supplies a **received** voice signal to the transistor(Q21). An operation amplifier(U1B) inverts the output signal of the operation amplifier(U1A) and inputs it to the transistor(Q31). Resistors(R17,R18) determine the amplification of the operation amplifier(U1B) as a unit gain of 1. Resistors(R19,R16) adjust the **receiving** gain of the operation amplifier(U1A). Capacitors(C1,C2) connect the outputs of the operation amplifiers(U1A,U1B) to the bases of the transistors(Q31Q21) respectively. A bias resistor(R3) prevents the transistors(Q3,Q31)(Q2,Q21) from operating in an interruption area when there is no AC load or DC load between the **tip** terminal and the **ring** terminal. Current/voltage conversion resistors(R1,R2) are provided to detect call current. Bridge resistors(R4-R7) compare the voltages detected by the resistors(R1,R2). A capacitor(C4) combines the AC impedance between the **ring** terminal and the power source with a

low impedance.
pp; 1 DwgNo 1/10
Title Terms: SUBSCRIBER; INTERFACE; CIRCUIT; FULL; ELECTRONIC; SWITCH; SYSTEM
Derwent Class: W01
International Patent Class (Main): H04M-003/30
File Segment: EPI

13/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011446570 **Image available**
WPI Acc No: 1997-424477/199739
XRPX Acc No: N97-353634
Loopback testing method for telephone subscriber line interface circuit **- connects current sources to each of** tip **and** ring **circuits, and conducts loopback test when telephone is on-hook and is successful when current from current sources simulates switch-hook detection**
Patent Assignee: HARRIS CORP (HARO)
Inventor: COTREAU G M; LUDEMAN C; WHITNEY D K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5659570	A	19970819	US 95380411	A	19950130	199739	B

Priority Applications (No Type Date): US 95380411 A 19950130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5659570	A		7		

Abstract (Basic): US 5659570 A
The method involves connecting separate current sources to each of the **tip** and **ring** circuits from which switch-hook is detected in the **subscriber line interface circuit** (SLIC). The method then evaluates whether a loopback test of the SLIC is successful by using current from the current sources in a switch-hook detection circuit of the SLIC.
Preferably current values are selected for the current sources that are separated by an amount sufficient to indicate switch-hook detection when connected. A successful loopback test is indicated with a switch-hook detection. Each of the separate current sources are preferably input to an input of a different one of several current amplifiers of the SLIC. Preferably the SLIC includes a ground key detect circuit that indicates whether the **ring** circuit is connected to ground.
USE/ADVANTAGE - E.g. for SLIC that may be used for on-hook **transmission** . Provides switch-hook detection indication. Allows loopback detection to be integrated into SLIC **IC** .
Dwg.3/3
Title Terms: LOOPBACK; TEST; METHOD; TELEPHONE; SUBSCRIBER; LINE; INTERFACE ; CIRCUIT; CONNECT; CURRENT; SOURCE; **TIP** ; **RING** ; CIRCUIT; CONDUCTING; LOOPBACK; TEST; TELEPHONE; ON-HOOK; SUCCESS; CURRENT; CURRENT; SOURCE; SIMULATE; SWITCH; HOOK; DETECT
Index Terms/Additional Words: **SLI CLoo**
Derwent Class: W01
International Patent Class (Main): H04M-001/24
International Patent Class (Additional): H04M-001/00
File Segment: EPI

13/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010581880 **Image available**
WPI Acc No: 1996-078833/199609
XRPX Acc No: N96-065581
Telephone subscriber line interface circuit **for four-wire** transmission **path - has independent two-wire impedance matching correction from** transmission **path, with hybrid circuitry having synthesised impedance which is grounded for controlling 2-wire** return **loss**
Patent Assignee: HARRIS CORP (HARO)
Inventor: LUDEMAN C; WHITNEY D K
Number of Countries: 007 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 693846	A2	19960124	EP 95304364	A	19950621	199609	B
JP 8051651	A	19960220	JP 95154648	A	19950621	199617	
CN 1135136	A	19961106	CN 95107654	A	19950623	199803	

Priority Applications (No Type Date): US 94264978 A 19940624
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 693846	A2	E	10	H04M-003/00	
Designated States (Regional): DE FR GB IT SE					
JP 8051651	A		9	H04Q-003/42	
CN 1135136	A			H04M-019/00	

Abstract (Basic): EP 693846 A
The SLIC subscriber line **integrated circuit** is connected between a 2-wire and a 4-wire **transmission** path, and has a combiner for mixing a **receive** signal current with **tip** and **ring** signal currents. An impedance matching circuit is referenced to ground through a an impedance which is preselected to approximate the anticipated impedance of a 2-wire **transmission** path to be connected to the SLIC.
A current mirror increases the gain of the combiner in inverse relation to the value of the impedance, and mutually independent elements adjust the 4-wire **transmission** signal gain, the 4-wire **receive** signal gain and the 2-wire impedance matching circuit.
ADVANTAGE - Enables impedance matching and trans-hybrid echo cancellation in **IC** within SLIC circuitry.
Dwg.5/6
Title Terms: TELEPHONE; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; FOUR; WIRE; **TRANSMISSION** ; PATH; INDEPENDENT; TWO; WIRE; IMPEDANCE; MATCH; CORRECT; **TRANSMISSION** ; PATH; HYBRID; CIRCUIT; SYNTHESIS; IMPEDANCE; GROUNDED; CONTROL; WIRE; **RETURN** ; LOSS
Index Terms/Additional Words: **SLIC**
Derwent Class: W01; W02
International Patent Class (Main): H04M-003/00; H04M-019/00; H04Q-003/42
International Patent Class (Additional): H04B-003/03; H04B-003/23
File Segment: EPI

13/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010383745 **Image available**
WPI Acc No: 1995-285059/199538
XRPX Acc No: N95-217063
Communication system metering signal generator and level control signal - has subscriber line interface circuit **and subscriber line, including integrated** semiconductor **device, having metered signal input and output operatively coupled to subscriber line**
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: MILLER M L; NAIR V V; RAMIREZ S; ZHOU Y

Number of Countries: 016 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 668687	A1	19950823	EP 95300281	A	19950118	199538	B
US 5452345	A	19950919	US 94184564	A	19940121	199543	
JP 8037564	A	19960206	JP 956586	A	19950119	199615	

Priority Applications (No Type Date): US 94184564 A 19940121
Cited Patents: 3.Jnl.Ref; EP 145038; FR 2563957
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 668687	A1	E	24	H04M-015/00	
Designated States (Regional): AT BE DE DK ES FR GB GR IE IT LU NL PT SE					
US 5452345	A		21	H04M-015/00	
JP 8037564	A		17	H04M-015/00	

Abstract (Basic): EP 668687 A

The signal generator has a metering signal generator (50) coupled to the metering signal input (23). The signal is injected on the subscriber line (20) through the integrated **semiconductor** device (23A). A program input (51) is coupled to the metering signal generator and **receives** a factor which is related to a first parameter of the metering signal.

The communication system (10) includes a subscriber line audio-processing circuit, a SLAC device (subscriber line audio processing circuit), which is (12) coupled to the **subscriber line interface circuit** (SLIC). The metering signal generator is integrated with the SLAC device. The generator includes a sine wave generator (90), having a sine wave output and a first multiplier (53) having a first input (53A) and a second input (53B). The first input is coupled with the sine wave output, and the second input is coupled with the program input (51).

ADVANTAGE - Reduces echo or reflection caused by variable impedance of subscriber lines in telephone communication systems.

Dwg.2/11

Title Terms: COMMUNICATE; SYSTEM; METER; SIGNAL; GENERATOR; LEVEL; CONTROL; SIGNAL; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; SUBSCRIBER; LINE; INTEGRATE ; **SEMICONDUCTOR** ; DEVICE; METER; SIGNAL; INPUT; OUTPUT; OPERATE; COUPLE; SUBSCRIBER; LINE
Derwent Class: W01
International Patent Class (Additional): H04M-003/00; H04M-015/38
File Segment: EPI

13/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010013809 **Image available**
WPI Acc No: 1994-281520/199435
XRPX Acc No: N94-221914

Subscriber line interface circuit **having reduced power dissipation when loop impedance is low - has pair of differential transconductance amplifiers to drive** tip **and** ring **lines of telephone exchange**

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: APFEL R J
Number of Countries: 015 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 615375	A2	19940914	EP 94300961	A	19940210	199435	B
JP 6303655	A	19941028	JP 9438281	A	19940309	199503	
US 5428682	A	19950627	US 9331785	A	19930312	199531	
EP 615375	B1	20010829	EP 94300961	A	19940210	200150	
DE 69428068	E	20011004	DE 628068	A	19940210	200166	

EP 94300961 A 19940210

Priority Applications (No Type Date): US 9331785 A 19930312
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 615375	A2	E	10	H04M-019/00	
Designated States (Regional): BE DE DK ES FR GB GR IE IT LU NL PT SE					
JP 6303655	A		10	H04Q-003/42	
US 5428682	A		11	H04M-019/00	
EP 615375	B1	E		H04M-019/00	
Designated States (Regional): BE DE DK ES FR GB GR IE IT LU NL PT SE					
DE 69428068	E			H04M-019/00	Based on patent EP 615375

Abstract (Basic): EP 615375 A

The interface circuit has an input circuit for **receiving** voice signals from a telephone exchange. One driver circuit drives a **tip** line of a telephone subscriber. Another driver circuit is coupled to the input circuit for driving a **ring** line of the subscriber loop, and both drivers **receive** power having two reference voltage terminals.

A resistor is coupled between the output of the second output driver and the second reference voltage terminal. Both output driver circuits comprise operational amplifiers, configured as differential transconductance amplifiers.

ADVANTAGE - Reduced heat generation, as resistor is produced off-chip, and current that otherwise flows through **ring** -line amplifier is diverted. Reduced space requirement.

Dwg.2/4

Title Terms: SUBSCRIBER; LINE; INTERFACE; CIRCUIT; REDUCE; POWER; DISSIPATE ; LOOP; IMPEDANCE; LOW; PAIR; DIFFERENTIAL; TRANSCONDUCTANCE; AMPLIFY; DRIVE; **TIP** ; **RING** ; LINE; TELEPHONE; EXCHANGE
Index Terms/Additional Words: **SLI CSub**
Derwent Class: U24; U25; W01
International Patent Class (Main): H04M-019/00; H04Q-003/42
File Segment: EPI

13/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008203603 **Image available**
WPI Acc No: 1990-090604/199012
Related WPI Acc No: 1984-312176
XRPX Acc No: N90-070005

Balanced signal transmission **system - has two operational amplifiers and differential amplifier connected to two-wire subscriber line and four-wire line of exchange**

Patent Assignee: SIEMENS AG (SIEI)
Inventor: MINCH M L; WAGNER T W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4897871	A	19900130	US 8731336	A	19870326	199012	B

Priority Applications (No Type Date): US 8731336 A 19870326; US 80137810 A 19800404; US 82350028 A 19820218; US 84627243 A 19840702
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4897871	A		11		

Abstract (Basic): US 4897871 A

The hybrid arrangement has two operational amplifier plus a differential amplifier connected together. The non-inverting input of the first operational amplifier is connected to a first reference

voltage and the output of this amplifier is connected to one wire of a two-wire subscriber line, and to the inverting input of the amplifier. The non-inverting input of the second operational amplifier is connected to a second reference voltage and to the **receiving** branch of a four-wire line.

The output of the second operational amplifier is connected to the other wire of the two-wire subscriber line, the inverting input and the inverting input of the first operational amplifier. Each of the two inputs of the differential amplifier are connected to one wire of the two-wire subscriber line and to the output of that operational amplifier which is connected to the other wire. The output or the differential amplifier is connected to the **transmitting** branch of the four-wire line of the exchange.

USE/ADVANTAGE - **Subscriber line interface circuit** telecommunications exchange. Suitable for implementation in **integrated circuit** form.

6/7

Title Terms: BALANCE; SIGNAL; **TRANSMISSION** ; SYSTEM; TWO; OPERATE; AMPLIFY ; DIFFERENTIAL; AMPLIFY; CONNECT; TWO; WIRE; SUBSCRIBER; LINE; FOUR; WIRE ; LINE; EXCHANGE
Derwent Class: W01
International Patent Class (Additional): H04M-003/22
File Segment: EPI

13/5/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008020484 **Image available**
WPI Acc No: 1989-285596/198939
XRPX Acc No: N89-218024

Semiconductor subscriber line interface circuit **- has thermally responsive sensor mounted in heat-relationship with resistive loop in subscriber loop**

Patent Assignee: ITEC INC (ITEC-N)
Inventor: HALBIG W A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4856059	A	19890808	US 87120067	A	19871113	198939	B

Priority Applications (No Type Date): US 87120067 A 19871113
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4856059	A		9		

Abstract (Basic): US 4856059 A

The **subscriber line interface circuit** has battery feed resistors in series circuit with the **ring** and **tip** lines to increase the impedance encountered by a lightning-induced voltage spike to increase the survivability of the **semiconductor** circuit components. The battery supply voltage is increased to effect a commensurate increase in loop current, and the loop impedance is re-adjusted by appropriately configured operational amplifiers.

A thermally responsive sensor is mounted in a heat-conducting relationship with resistive elements in the subscriber loop with an increase in temperature representing an overcurrent situation, such as power line cross-over, and provides a control signal effective to disconnect the subscriber loop from interface circuit.

ADVANTAGE - Improved immunity to overvoltage conditions.

2/5

Title Terms: **SEMICONDUCTOR** ; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; THERMAL ; RESPOND; SENSE; MOUNT; HEAT; RELATED; RESISTOR; LOOP; SUBSCRIBER; LOOP
Index Terms/Additional Words: TELEPHONE

Derwent Class: W01
International Patent Class (Additional): H04M-001/74
File Segment: EPI

13/5/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004736915
WPI Acc No: 1986-240257/198637
XRPX Acc No: N86-179493
Telephone subscriber line interface circuit - **reduces energy consumption by output stages generating line voltage in listening mode**
Patent Assignee: THOMSON CSF (CSFC)
Inventor: DEFRETIN B; GUERIN M
Number of Countries: 009 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 194177	A	19860910	EP 86400297	A	19860211	198637	B
FR 2577737	A	19860822				198640	
JP 61228800	A	19861011	JP 8631762	A	19860215	198647	
US 4709388	A	19871124	US 86828691	A	19860212	198749	
CA 1240432	A	19880809				198836	
EP 194177	B	19890104				198902	
DE 3661671	G	19890209				198907	

Priority Applications (No Type Date): FR 852249 A 19850215
Cited Patents: 3.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 194177	A	F	10		
Designated States (Regional): DE FR GB IT NL SE					
EP 194177	B	F			
Designated States (Regional): DE FR GB IT NL SE					

Abstract (Basic): EP 194177 B

In a high-voltage **integrated circuit** , speech or ringing signals are applied to a phase shifter feeding two preamplifiers with separate push-pull output stages connected to the line conductors. When the interface is in listening mode, current sources are switched out and the preamplifiers are isolated so that the output stages are transformed into fixed line voltage generators.

A differential voltage is supplied which approximates to the difference between the high-voltage circuit supply potentials. The interface remains capable of measuring the line current (to detect a **receiver** off-hook) and absorbing longitudinal current from the line.

ADVANTAGE - 70% of functions of high-voltage circuit are no longer su-plied, but capacity for longitudinal current absorption is retained.

(10pp Dwg.No.6/6

Title Terms: TELEPHONE; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; REDUCE; ENERGY; CONSUME; OUTPUT; STAGE; GENERATE; LINE; VOLTAGE; LISTENER; MODE
Derwent Class: W01
International Patent Class (Additional): H04M-007/00; H04M-019/00; H04Q-001/28; H04Q-003/72
File Segment: EPI

20/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04131044 **Image available**
LIGHT **SUBSCRIBER LINE INTERFACE CIRCUIT**

PUB. NO.: 05-122744 [JP 5122744 A]
PUBLISHED: May 18, 1993 (19930518)
INVENTOR(s): IGUCHI HIROTO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-311639 [JP 91311639]
FILED: October 30, 1991 (19911030)
INTL CLASS: [5] H04Q-003/42; H04B-010/24
JAPIO CLASS: 44.4 (COMMUNICATION -- Telephone); 44.2 (COMMUNICATION -- **Transmission** Systems)
JAPIO KEYWORD: R012 (OPTICAL FIBERS)
JOURNAL: Section: E, Section No. 1428, Vol. 17, No. 494, Pg. 99, September 07, 1993 (19930907)

ABSTRACT

PURPOSE: To effectively discriminate whether or not a **transmitting** call and a **receiving** call occur simultaneously.
CONSTITUTION: A first light **transmitting receiving** means 21 and a second light **transmitting receiving** means 22 having directivity couplers 4 and 10 connected mutually through a light subscriber line are equipped, and respective light **transmitting receiving** means 21 and 22 is provided with optic/electric converting parts 6 and 12 for converting a light signal related to a sent **transmitting** call or a **receiving** call to an electrical signal and electric/optic converting parts 3 and 9 for converting the electric signal related to the **receiving** call or the **transmitting** call to the light signal. To the input step of the electric-light converting parts 3 and 9 of the first light **transmitting receiving** means 21, a selecting circuit 2 to input the output of an oscillator 1 and a **transmitting** signal sent from an external part and select and output either of them is equipped. To the output step of the optic/electric converting part 12 at the second light **transmitting receiving** means 22, a **signal identifying** circuit 11 to **identify** a **signal** from the first **transmitting receiving** means 21 is equipped.

20/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015029189 **Image available**
WPI Acc No: 2003-089706/200308
XRPX Acc No: N03-070737
Loop voltage measurement circuit for subscriber line interface circuit **, generates current fractionally and proportional to current output from current node for producing differential** tip - ring **voltage**
Patent Assignee: INTERSIL CORP (INTE-N)
Inventor: ENRIQUEZ L E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6469519	B1	20021022	US 2000686324	A	20001011	200308	B

Priority Applications (No Type Date): US 2000686324 A 20001011
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6469519	B1		7	G01R-023/20	

Abstract (Basic): US 6469519 B1

NOVELTY - A **voltage detector** coupled to **tip** and **ring** ports of telephone line pair, is operated at current output node for producing output current representing differential **tip - ring voltage** and **detector** internal characteristic. A generator generates current fractionally and proportional to produced current, and **voltage** associated with **detector** internal characteristics detector for producing differential **tip - ring** voltage.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for single ended output deriving method.

USE - For **subscriber line interface circuit** (SLIC).

ADVANTAGE - Single ended output voltage is produced precisely by producing differential **tip - ring** voltage efficiently and power consumption is also reduced.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the loop **voltage detection** circuit.

pp; 7 DwgNo 1/1

Title Terms: LOOP; VOLTAGE; MEASURE; CIRCUIT; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; GENERATE; CURRENT; FRACTION; PROPORTION; CURRENT; OUTPUT; CURRENT; NODE; PRODUCE; DIFFERENTIAL; **TIP** ; **RING** ; VOLTAGE

Derwent Class: S01; W01

International Patent Class (Main): G01R-023/20

International Patent Class (Additional): G01R-027/00; G01R-031/02

File Segment: EPI

20/5/3 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014867835 **Image available**

WPI Acc No: 2002-688541/200274

Apparatus for saving power of wll terminal and method therefor

Patent Assignee: CURITEL INC (CURI-N)

Inventor: KIM G B

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002037872	A	20020523	KR 200067802	A	20001115	200274	B

Priority Applications (No Type Date): KR 200067802 A 20001115

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002037872	A		1	H04M-019/00	

Abstract (Basic): KR 2002037872 A

NOVELTY - An apparatus for saving a power of a WLL(Wireless Local Loop) terminal and a method therefor are provided to increase a standby time of the WLL terminal by selectively controlling the driving of an SLIC(**Subscriber Line Interface Circuit**) of the WLL terminal according to a hook state of a wired telephone and the sensing of a **receiving ring** and saving a consumption current.

DETAILED DESCRIPTION - A hook sensing unit(300) connects to a **tip** terminal of an SLIC(200) for interfacing a wired/wireless signal between a wired telephone(100) and a BTS(Base Transceiver Station) and senses a hook state. A control unit(500) generates a power control signal for controlling a driving power of the SLIC(200) according to a hook state signal and a **receiving ring sensing signal** outputted from the hook sensing unit(300) or a **receiving ring sensing** unit. A **power** switching unit(400) supplies or blocks the driving power to the SLIC(200) according to the power control signal outputted from the control unit(500).

pp; 1 DwgNo 1/10

Title Terms: APPARATUS; SAVE; POWER; TERMINAL; METHOD

Derwent Class: W01

International Patent Class (Main): H04M-019/00

File Segment: EPI

20/5/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014854529 **Image available**
WPI Acc No: 2002-675235/200272
XRPX Acc No: N02-533888
Ringing current limiting method e.g. for SLIC, involves sensing **value of ringing** current **and comparing it with maximum value to detect when sensed value exceeds maximum value**
Patent Assignee: TELEFONAKTIEBOLAGET ERICSSON L M (TELF)
Inventor: EMERICKS A; HELLBERG H
Number of Countries: 100 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200273936	A2	20020919	WO 2002SE413	A	20020307	200272	B

Priority Applications (No Type Date): SE 2001802 A 20010309
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200273936	A2	E	12	H04M-000/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): WO 200273936 A2
NOVELTY - The method involves sensing a value of the ringing current and comparing (4) it with the maximum value to detect when the sensed value exceeds the maximum value (15). In response to that the sensed value exceeds the maximum value, a signal which is proportional to the different between the sensed and the maximum value is generated. The ringing current is attenuated in response to the signal so that its peak value is kept equal to or below the maximum value.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for an arrangement for limiting a ringing current in a SLIC
USE - For **subscriber line interface circuits** (SLIC). For ringing current limitation in SLICs
ADVANTAGE - Limits ringing current to value just above desired ringing current and reduces the off-hook current or fault condition current and keeps it at the desired level until the ringing signal is turned off.
DESCRIPTION OF DRAWING(S) - The figure shows schematically shows a SLIC1 connected to wires A and B of a two wire **transmission** line to a subscriber station.
Comparator (4)
Maximum value (15)
pp; 12 DwgNo 1/2
Title Terms: **RING** ; CURRENT; LIMIT; METHOD; SLIC; SENSE; VALUE; **RING** ; CURRENT; COMPARE; MAXIMUM; VALUE; DETECT; SENSE; VALUE; MAXIMUM; VALUE
Derwent Class: U24; W01; W02
International Patent Class (Main): H04M-000/00
File Segment: EPI

20/5/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014283916 **Image available**
WPI Acc No: 2002-104617/200214
Structure and method for using generic pstn telephone in soho internet phone gateway
Patent Assignee: REDNIX CO LTD (REDN-N)
Inventor: KIM S H; LEE B G; MOK G S; PARK S H; SHIN H S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001079469	A	20010822	KR 200144278	A	20010723	200214	B

Priority Applications (No Type Date): KR 200144278 A 20010723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001079469	A		1	H04L-012/66	

Abstract (Basic): KR 2001079469 A
NOVELTY - A structure and method for using a generic PSTN telephone in a SOHO Internet phone gateway is provided to offer the calling and **receiving** functions of both an Internet phone and a PSTN telephone, regardless of a connected state, by confirming a connection state according to suitable procedures.
DETAILED DESCRIPTION - **Tip** / **ring** terminals(21) are connected with a subscriber line of a PSTN telephone office. A terminal(22) is to connect a generic telephone. An AC input terminal(23) supplies system power. A relay(24) is provided for connection transfer when a user attempts an Internet call and a PSTN through the generic telephone. A DC power supplier supplies DC **power** . A loop **detector** (26) monitors the loop of the call current of a PSTN trunk. A **ring** detector(27) **detects** a **ring signal** . A SLIC(**Subscriber Line Interface Circuit**)(28) supplies call current and **ring** signals for Internet calls. A relay driver(29) drives a signal transfer relay.
pp; 1 DwgNo 1/10
Title Terms: STRUCTURE; METHOD; PSTN; TELEPHONE; TELEPHONE; GATEWAY
Derwent Class: W01
International Patent Class (Main): H04L-012/66
File Segment: EPI

20/5/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014240774 **Image available**
WPI Acc No: 2002-061474/200208
XRPX Acc No: N02-045597
Subscriber line interface termination circuit has voice band filter which isolates voice band return **loss signal from data band signal**
Patent Assignee: MITEL CORP (MTLC); GEISS R (GEIS-I); LUNG J (LUNG-I)
Inventor: GEISS R; LUNG J
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010033651	A1	20011025	US 2001832980	A	20010412	200208	B
DE 10120197	A1	20011122	DE 1020197	A	20010424	200208	
FR 2808152	A1	20011026	FR 20015550	A	20010425	200208	
GB 2362063	A	20011107	GB 200010075	A	20000425	200208	
CN 1321037	A	20011107	CN 2001109598	A	20010424	200216	

Priority Applications (No Type Date): GB 200010075 A 20000425
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010033651	A1		6	H04M-001/00	
DE 10120197	A1			H04M-011/06	
FR 2808152	A1			H04L-025/14	

GB 2362063 A H04B-003/23
CN 1321037 A H04M-003/42

Abstract (Basic): US 20010033651 A1

NOVELTY - A voice band **return** loss circuit (114) monitors the voice and data **signals** **detected** at a **transmission** medium connection point and generates a voice band **return** signal. A voice band filter (113) connected to the **return** loss circuit, isolates the voice band **return** loss signal from the data band signal.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Trans hybrid component and near end echo canceling system in communications system;

(b) Communication system interface terminating method;

(c) Trans hybrid component and near end echo canceling method

USE - For use in connecting broadband voice and data signals to telephone networks e.g. for interfacing a DSL analog front end circuit to a subscriber line in the presence of voice band (DC-4000 Hz) signal.

ADVANTAGE - Incorporates a voice band filter to minimize the impact on the data band signal. Hence provides circuit with ability to reduce far end echo in the voice band and allows for good voice band performance as well as a simpler data band **receive** circuit.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of universal **subscriber** **line** **interface** **circuit** (SLSC).

Voice band filter (113)

Voice band **return** loss circuit (114)

pp; 6 DwgNo 1/1

Title Terms: SUBSCRIBER; LINE; INTERFACE; TERMINATE; CIRCUIT; VOICE; BAND; FILTER; ISOLATE; VOICE; BAND; **RETURN** ; LOSS; SIGNAL; DATA; BAND; SIGNAL
Derwent Class: W01
International Patent Class (Main): H04B-003/23; H04L-025/14; H04M-001/00; H04M-003/42; H04M-011/06
International Patent Class (Additional): H04B-003/20; H04L-005/06; H04M-003/00; H04M-009/00
File Segment: EPI

20/5/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014103849 **Image available**
WPI Acc No: 2001-588063/200166
Subscriber access subsystem having automatic channel assignment function in wll system and method for automatically assigning channels
Patent Assignee: MERCURY CORP (MERC-N)
Inventor: LEE G D
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001038210	A	20010515	KR 9946096	A	19991022	200166	B
KR 314569	B	20011115	KR 9946096	A	19991022	200240	

Priority Applications (No Type Date): KR 9946096 A 19991022
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001038210	A		1	H04Q-007/20	
KR 314569	B			H04Q-007/20	Previous Publ. patent KR 2001038210

Abstract (Basic): KR 2001038210 A

NOVELTY - A subscriber access subsystem having an automatic channel assignment function in a WLL(Wireless Local Loop) system and a method for automatically assigning channels are provided to prevent the interruption of communication service by making a subscriber access

subsystem recognize the position of an SLIC(**Subscriber Line Interface Circuit**) board or an SIO(Serial Input Output) board so that time slots can automatically be allocated.

DETAILED DESCRIPTION - An antenna(11) **transmits** and/or **receives** radio signals. A **transmit - receive** processing part(12) converts a **received** analog signal into a digital signal or a digital signal to **send** into an analog signal. A modem(13) modulates or demodulates the data **transmitted** or **received** . A switching part(14) classifies the signals supplied from the modem(13) by time slots and outputs them to a serial connection part(15) and a port connection part(16). The serial connection part(15) consists of a data conversion part(151), a DPRAM(152) and a time slot interface part(153). The data conversion part(151) converts serial data into PCM data or PCM data into serial data. The DPRAM(152) is provided for message exchange between the serial connection part(15) and a processor(17) in order to confirm the allocation of time slots. The time slot interface part(153) outputs the PCM data, inputted from the data conversion part(151), to the switching part(14) by allocating a time slot. The port connection part(16) is comprised of a signal interface processing part(161) and a CODEC(162). The signal interface processing part(161) generates a **ring signal** , a **detects** a DTMF **signal** , and converts an input PCM signal into a voice signal or a facsimile signal. The CODEC(162) encodes or decodes input data.

pp; 1 DwgNo 1/10

Title Terms: SUBSCRIBER; ACCESS; SUBSYSTEM; AUTOMATIC; CHANNEL; ASSIGN; FUNCTION; SYSTEM; METHOD; AUTOMATIC; ASSIGN; CHANNEL

Derwent Class: W01

International Patent Class (Main): H04Q-007/20

File Segment: EPI

20/5/8 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011769461 **Image available**

WPI Acc No: 1998-186371/199817

XRPX Acc No: N98-148214

Subscriber line interface circuit **for electronic switching system - has CPU which outputs control signal by which switch output terminal, which outputs PB signal, and switch input terminal which inputs** transmitted **signal, is connected**

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10042321	A	19980213	JP 96197903	A	19960726	199817	B

Priority Applications (No Type Date): JP 96197903 A 19960726

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10042321	A		8	H04Q-001/45	

Abstract (Basic): JP 10042321 A

The circuit (SLIC) has a switch (23) whose input terminal is connected to an output terminal according to a control signal from a CPU (11). A **transmitted** signal is input via the input terminal of the switch.

A PB signal is output to a PB signal **receiver** (PBR0-PBRn) via the output terminal of the switch. The CPU outputs the control **signal** according to a **detection signal** from a call monitoring unit which monitors the operation of a telephone.

ADVANTAGE - Enables efficient usage of PB signal **receiver** by preventing signal loss in communication channel.

Dwg.1/6

Title Terms: SUBSCRIBER; LINE; INTERFACE; CIRCUIT; ELECTRONIC; SWITCH; SYSTEM; CPU; OUTPUT; CONTROL; SIGNAL; SWITCH; OUTPUT; TERMINAL; OUTPUT; SIGNAL; SWITCH; INPUT; TERMINAL; INPUT; **TRANSMIT** ; SIGNAL; CONNECT
Derwent Class: W01
International Patent Class (Main): H04Q-001/45
File Segment: EPI

20/5/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011394397 **Image available**
WPI Acc No: 1997-372304/199734
XRPX Acc No: N97-309214
Longitudinal current sensing **and compensating circuit -** senses voltage **difference between reference and longitudinal voltages in subscriber loop and provides currents to current amplifiers that feed** tip **and** ring **lines of subscriber loop, to compensate for longitudinal currents**
Patent Assignee: HARRIS CORP (HARO)
Inventor: ENRIQUEZ L E; USCATEGUI G J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5649009	A	19970715	US 94340342	A	19941114	199734	B

Priority Applications (No Type Date): US 94340342 A 19941114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5649009	A		7		

Abstract (Basic): US 5649009 A
The circuit involves a subscriber loop, in which the **tip** terminal is connected to a first current amplifier and the **ring** terminal is connected to a second current amplifier. The circuit includes a longitudinal amplifier (32) for **sensing** a **voltage** difference between a reference voltage and a longitudinal voltage, in the subscriber loop. The amplifier provides two current differences of opposite polarity to each of the current amplifiers (22).
The magnitudes of the current differences are equal and proportional to the voltage difference. Preferably the longitudinal amplifier comprises a pair of current mirrors, with gains that are greater than one, each for providing currents of the same magnitude. The longitudinal amplifier preferably further includes a pair of transistors with common emitters for **receiving** a common operating current, and with collectors that provide inputs to the current mirrors.
USE/ADVANTAGE - E.g. for avoiding unwanted longitudinal (common mode) currents in subscriber loop of telephone system. Uses differential current approach to increase power savings per chip area. Applies two pairs of matched currents to two pairs of matched resistors, at current amplifiers to improve operating precision. Reduces system noise in **subscriber line interface circuit** .
Dwg.2/3
Title Terms: LONGITUDE; CURRENT; SENSE; COMPENSATE; CIRCUIT; SENSE; VOLTAGE ; DIFFER; REFERENCE; LONGITUDE; VOLTAGE; SUBSCRIBER; LOOP; CURRENT; CURRENT; AMPLIFY; FEED; **TIP** ; **RING** ; LINE; SUBSCRIBER; LOOP; COMPENSATE ; LONGITUDE; CURRENT
Derwent Class: W01; W02
International Patent Class (Main): H04M-019/00
File Segment: EPI

20/5/10 (Item 9 from file: 350)

010545383 **Image available**
WPI Acc No: 1996-042336/199605
XRPX Acc No: N96-035501

Isolation circuit connected between SLIC and telephone ringer generator - uses gain blocking device to provide signal gain when ringer generator is not being used and high impedance when ringer signal is present

Patent Assignee: HARRIS CORP (HARO)
Inventor: COTREAU G M; COTREAU G W

Number of Countries: 009 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2290921	A	19960110	GB 9513091	A	19950627	199605	B
JP 8051652	A	19960220	JP 95159495	A	19950626	199617	
US 5515417	A	19960507	US 94267436	A	19940629	199624	
US 5515434	A	19960507	US 94267434	A	19940629	199624	
US 5517565	A	19960514	US 94269133	A	19940630	199625	
EP 760576	A1	19970305	EP 95306029	A	19950830	199714	N
CN 1136743	A	19961127	CN 95107776	A	19950628	199805	
CN 1367603	A	20020904	CN 95107776	A	19950628	200281	
			CN 2001135941	A	19950628		
CN 1365228	A	20020821	CN 95107776	A	19950628	200281	
			CN 2001135940	A	19950628		

Priority Applications (No Type Date): US 94269133 A 19940630; US 94267434 A 19940629; US 94267436 A 19940629; EP 95306029 A 19950830
Cited Patents: 2.Jnl.Ref; EP 520171; JP 60170308; US 4203012; WO 8810542
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2290921	A		28	H04M-019/02	
JP 8051652	A		14	H04Q-003/42	
US 5515417	A		9	H04M-003/08	
US 5515434	A		10	H04M-001/76	
US 5517565	A		10	H04M-003/02	
EP 760576	A1	E	21	H04M-019/02	
Designated States (Regional): AT DE FR IT SE					
CN 1136743	A			H04M-019/00	
CN 1367603	A			H04M-003/22	Div ex application CN 95107776
CN 1365228	A			H04M-019/00	Div ex application CN 95107776

Abstract (Basic): GB 2290921 A

The circuit for a telephone system has a **subscriber line interface circuit** (SLIC) with **tip** and **ring** circuits electrically interconnecting the SLIC and the telephone. A ringer generator generates a ringer signal. A switch selectively applies the ringer signal to the **tip** and **ring** paths. A selectively operable gain setting blocking device isolates the SLIC from the ringer signal.

Pref., the gain setting has an amplifier capable of going into a tri-state mode. The output of the amplifier has a high impedance when in the tri-state mode. The amplifier selectively operates to drive the **tip** path and the **ring** path. A current source is used too drive the amplifier.

USE/ADVANTAGE - Isolates SLIC from ringer generator without using relay which may distort signal on telephone line. SLIC two wire **return** loss reduced by impedance matching. Prevents two-wire echo.

Dwg.3/10

Title Terms: ISOLATE; CIRCUIT; CONNECT; SLIC; TELEPHONE; **RING** ; GENERATOR; GAIN; BLOCK; DEVICE; SIGNAL; GAIN; **RING** ; GENERATOR; HIGH; IMPEDANCE; **RING** ; SIGNAL; PRESENT
Derwent Class: W01
International Patent Class (Main): H04M-001/76; H04M-003/02; H04M-003/08; H04M-003/22; H04M-019/00; H04M-019/02; H04Q-003/42
International Patent Class (Additional): H04M-003/42; H04M-007/00;

H04M-009/00; H04M-009/08
File Segment: EPI

20/5/11 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010271348 **Image available**
WPI Acc No: 1995-172603/199523
Related WPI Acc No: 1995-180417
XRPX Acc No: N95-135325

Subscriber line interface circuit **between four wire line and two wire line - has correlator and control circuit connected for** receiving **longitudinal signal and transversal signal corresp. to differential signal** received **on terminal of two wire interface from two wire line**

Patent Assignee: TELEFONAKTIEBOLAGET ERICSSON L M (TELF)
Inventor: ERIKSSON G A; MEYER J G
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2283888	A	19950517	GB 9420873	A	19941017	199523	B
FR 2712448	A1	19950519	FR 9413364	A	19941108	199525	
SE 9303689	A	19950510	SE 933689	A	19931109	199530	
CA 2135321	A	19950510	CA 2135321	A	19941108	199532	
SE 501975	B	19950703	SE 933689	A	19931109	199532	
JP 7303265	A	19951114	JP 94273982	A	19941108	199603	
US 5526425	A	19960611	US 94334075	A	19941104	199629	
GB 2283888	B	19980708	GB 9420873	A	19941017	199829	

Priority Applications (No Type Date): SE 933689 A 19931109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2283888	A		19	H04B-003/03	
JP 7303265	A		9	H04Q-003/42	
US 5526425	A		9	H04M-019/00	
FR 2712448	A1			H04M-009/00	
SE 9303689	A			H04B-001/58	
CA 2135321	A			H04M-011/00	
SE 501975	B			H04B-001/58	
GB 2283888	B			H04B-003/03	

Abstract (Basic): GB 2283888 A

The circuit includes a correlator and control circuit (32, 34, 36) connected for **receiving** a longitudinal signal (Vt) corresp. to a differential signal **received** on the terminal of two wire interface from the two wire line. The correlator and control circuit includes a circuit (32) for creating a correction signal (33) being a measure of the correlation between the longitudinal signal and the transversal signal.

The circuit for creating a correction signal (33) being a measure of the correlation between the longitudinal signal and the transversal signal, is connected for using this correction **signal** to **adaptively** control the amplifications in feed back loops (26,14, 18; 28,16, 20) so as to minimize the correlation between the longitudinal and transversal signals.

ADVANTAGE - Adjustment of longitudinal balance to max. may be performed continuously when circuit is in operation.

Dwg.1/10

Title Terms: SUBSCRIBER; LINE; INTERFACE; CIRCUIT; FOUR; WIRE; LINE; TWO; WIRE; LINE; CORRELATE; CONTROL; CIRCUIT; CONNECT; **RECEIVE** ; LONGITUDE; SIGNAL; TRANSVERSE; SIGNAL; CORRESPOND; DIFFERENTIAL; SIGNAL; **RECEIVE** ; TERMINAL; TWO; WIRE; INTERFACE; TWO; WIRE; LINE
Derwent Class: W01
International Patent Class (Main): H04B-001/58; H04B-003/03; H04M-009/00;

H04M-011/00; H04M-019/00; H04Q-003/42
International Patent Class (Additional): H03M-003/00; H04Q-001/00
File Segment: EPI

20/5/12 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009909859 **Image available**
WPI Acc No: 1994-177565/199422
XRPX Acc No: N94-139857
Telephone subscriber line interface for controlling output impedance - senses AC and DC variations in received **transmission signals, and provides feedback signals for controlling AC and DC output impedances**
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: SUSAK D M; TAKESHIAN T; WELTY D L
Number of Countries: 004 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 600175	A1	19940608	EP 93115426	A	19930924	199422	B
US 5329585	A	19940712	US 92983197	A	19921130	199427	

Priority Applications (No Type Date): US 92983197 A 19921130
Cited Patents: BE 903082; EP 112731; EP 169706
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 600175	A1	E	9	H04M-019/00	
Designated States (Regional): DE FR GB					
US 5329585	A		7	H04M-001/76	

Abstract (Basic): EP 600175 A
A **subscriber line interface circuit** (10) establishes AC and DC output impedances as seen by first (14) and second (12) **transmission** signals. The common mode and differential variations of both **transmission signals** are AC- **sensed** to provide common mode (56, 80) and differential feedback signals, which in turn control the AC output impedance.
The DC component of both **transmission** signals is blocked (24, 30), allowing downstream amplifiers to operate at reduced power supply potential. The DC variation of both **transmission signals** is **sensed** (110,142) to provide a DC feedback signal for controlling the DC output impedance.
USE/ADVANTAGE - Partic. for tele-metering and caller identification etc. Interfaces subscriber lines to telephone exchange network, using reduced operational amplifier supply voltage for reduced overall power consumption.
Dwg.1/1
Title Terms: TELEPHONE; SUBSCRIBER; LINE; INTERFACE; CONTROL; OUTPUT; IMPEDANCE; SENSE; AC; DC; VARIATION; **RECEIVE** ; **TRANSMISSION** ; SIGNAL; FEEDBACK; SIGNAL; CONTROL; AC; DC; OUTPUT; IMPEDANCE
Index Terms/Additional Words: **SLIC_TI P-RINGTeleph** ; **TIP - RING**
Derwent Class: W01
International Patent Class (Main): H04M-001/76; H04M-019/00
International Patent Class (Additional): H04M-007/04
File Segment: EPI

20/5/13 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009466244 **Image available**
WPI Acc No: 1993-159783/199320
XRPX Acc No: N93-122660

Telephone subscriber line interface circuit **- has differential amplifier with differential inputs coupled to** tip **and** ring **taps and output coupled to inputs of** tip **and** ring **feed amplifiers**

Patent Assignee: MOISIN M S (MOIS-I)
Inventor: MOISIN M S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CA 2077160	A	19930304	CA 2077160	A	19920828	199320	B

Priority Applications (No Type Date): US 91754453 A 19910903
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CA 2077160	A		38	H04M-019/00	

Abstract (Basic): CA 2077160 A

The d.c. supply uses **tip** and **ring** feed amplifiers (20, 30) to control energising d.c. at the **tip** and **ring** terminals (2, 3). **Tip** and **ring** feed resistor chains (21, 22; 31, 32) are respectively connected between the **tip** and **ring** terminals and outputs of the feed amplifiers. **Tip** and **ring** taps (23, 38) are located between the feed resistors in each chain.

A capacitor (11) and inductances (P) provide an a.c. terminating ipedance between the **tip** and **ring** taps. A differential amplifier (50) connected to the latter provides differential **voltage sensing** and compensation.

USE - Supplying energising current to subscribers appts. and coupling signals via subscriber pair.

Dwg.1/7

Title Terms: TELEPHONE; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; DIFFERENTIAL; AMPLIFY; DIFFERENTIAL; INPUT; COUPLE; **TIP** ; **RING** ; TAP; OUTPUT; COUPLE; INPUT; **TIP** ; **RING** ; FEED; AMPLIFY
Derwent Class: W01
International Patent Class (Main): H04M-019/00
File Segment: EPI

20/5/14 (Item 13 from file: 350)

009460573 **Image available**
WPI Acc No: 1993-154100/199319
XRPX Acc No: N93-117881

Remote subscriber control system for digital telephone line switching system - has transmitter **coupled to subscriber line interface, switch side** transmitter **coupled to switch and digital** transmission **path connecting** transmitters **so that multiplexed signals are** transmitted

Patent Assignee: FUJITSU LTD (FUIT)
Inventor: INOUE S; MATSUMOTO Y
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 541123	A2	19930512	EP 92119088	A	19921106	199319	B
JP 5130667	A	19930525	JP 91291590	A	19911107	199325	
EP 541123	A3	19940524	EP 92119088	A	19921106	199525	
US 5606605	A	19970225	US 92972005	A	19921105	199714	

Priority Applications (No Type Date): JP 91291590 A 19911107
Cited Patents: No-SR.Pub; 1.Jnl.Ref; EP 48129; GB 2083320; JP 59070395; US 4197427; US 4466095; US 5046067
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 541123	A2	E	20	H04Q-003/00	
US 5606605	A		17	H04M-003/00	

JP 5130667 A H04Q-003/60
EP 541123 A3 H04Q-003/00

Abstract (Basic): EP 541123 A

The control system comprises the remote subscriber **transmitter** (80) coupled to the subscriber line interface, and the switch side **transmitter** (70) coupled to the switch (1). The digital **transmission** path (45) connects the remote subscriber **transmitter** to the switch side **transmitter** so that multiplexed signals including speech signals and control signals are **transmitted** through the digital **transmission** path.

The side **transmitter** comprises a state change detection unit (81) to detect a change of state of the remote subscriber terminal, and a state storage unit for storing state information indicating its state when a change takes place. A dialling number specifying a called terminal is also stored (82).

ADVANTAGE - Remote subscriber control terminal can be effectively controlled and function for communications can be economically changed.

Dwg.5/12

Title Terms: REMOTE; SUBSCRIBER; CONTROL; SYSTEM; DIGITAL; TELEPHONE; LINE; SWITCH; SYSTEM; **TRANSMIT** ; COUPLE; SUBSCRIBER; LINE; INTERFACE; SWITCH; SIDE; **TRANSMIT** ; COUPLE; SWITCH; DIGITAL; **TRANSMISSION** ; PATH; CONNECT; **TRANSMIT** ; SO; MULTIPLEX; SIGNAL; **TRANSMIT**

Derwent Class: W01; W02

International Patent Class (Main): H04M-003/00; H04Q-003/00; H04Q-003/60

International Patent Class (Additional): H04Q-003/545; H04Q-011/04

File Segment: EPI

20/5/15 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009307612 **Image available**

WPI Acc No: 1993-001048/199301

XRPX Acc No: N93-000647

Off-hook detection circuit for subscriber line interface circuit **- has interface circuit between subscriber line and exchange which uses detector unit to recognise possible hook-off state and** sends **corresp. signal to exchange**

Patent Assignee: SGS THOMSON MICROELTRN SRL (SGSA); MARCIONI M L (MARC-I)

Inventor: SAVIOTTI V; SILIGONI M

Number of Countries: 023 Number of Patents: 012

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 520171	A1	19921230	EP 92107867	A	19920511	199301	B
BR 9202108	A	19930202	BR 922108	A	19920602	199309	
CA 2068971	A	19921226	CA 2068971	A	19920519	199316	
TW 199951	A	19930211	TW 92103655	A	19920512	199328	
JP 5167678	A	19930702	JP 92140551	A	19920601	199329	
CN 1068229	A	19930120	CN 92103695	A	19920515	199347	
US 5402484	A	19950328	US 92891548	A	19920529	199518	
IT 1248549	B	19950119	IT 91MI1748	A	19910625	199531	
EP 520171	B1	19970205	EP 92107867	A	19920511	199711	
DE 69217279	E	19970320	DE 617279	A	19920511	199717	
			EP 92107867	A	19920511		
KR 263659	B1	20000801	KR 9210462	A	19920617	200132	
CA 2068971	C	20020122	CA 2068971	A	19920519	200216	

Priority Applications (No Type Date): IT 91MI1748 A 19910625

Cited Patents: 01Jnl.Ref; CH 675803; EP 73462; US 4473719

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 520171	A1	E	9	H04M-019/02	

Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI LU MC NL

PT SE
BR 9202108 A H04M-003/22
CA 2068971 A H04M-003/22
TW 199951 A H04M-001/24
JP 5167678 A H04M-019/02
CN 1068229 A H04M-001/24
US 5402484 A 9 H04M-019/00
IT 1248549 B H04B-000/00
EP 520171 B1 E 12 H04M-019/02
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI LU MC NL
PT SE
DE 69217279 E H04M-019/02 Based on patent EP 520171
KR 263659 B1 H04M-003/14
CA 2068971 C E H04M-003/22

Abstract (Basic): EP 520171 A

The assembly comprises an interface circuit (3') between the telephone subscriber line (L) and exchange control apparatus. A supply circuit (5') includes a DC voltage source (UB) and a **ring** AC generator (AC') in series with each other. A switch-over unit (7), controlled by the exchange control apparatus, puts the telephone subscriber line through the interface circuit or the supply circuit.

Two resistances (RP and RP') of the same value are serially connected between one (B, A) of the telephone subscriber line (L) terminals, with the line connected to the supply circuit by the switch-over unit. A processor responsive to the current on the telephone line **isolates** the useful **signal** component (IT) from the **current** , **recognises** any DC component during the **ring** step and **sends** this recognition to the exchanges.

ADVANTAGE - **Senses** presence of direct **current** on line due to hooking-off even where it overlaps **alternate current** of possible **ring** signal. Requires no high accuracy resistors to recognise hook-off condition.

Dwg.2/5

Title Terms: OFF-HOOK; DETECT; CIRCUIT; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; INTERFACE; CIRCUIT; SUBSCRIBER; LINE; EXCHANGE; DETECT; UNIT; RECOGNISE; POSSIBILITY; HOOK; STATE; **SEND** ; CORRESPOND; SIGNAL; EXCHANGE
Derwent Class: W01
International Patent Class (Main): H04B-000/00; H04M-001/24; H04M-003/14; H04M-003/22; H04M-019/00; H04M-019/02
File Segment: EPI

20/5/16 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009090035 **Image available**
WPI Acc No: 1992-217455/199227
XRPX Acc No: N92-165134
Auto-equalising bidirectional-to-unidirectional hybrid network - has tone generator producing supervisory signal for receive **path used to monitor performance to balance network**
Patent Assignee: GLENAYRE ELECTRONICS LTD (GLEN-N); GLENAYRE ELECTRONICS INC (GLEN-N)
Inventor: CAESAR D D
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CA 2028016	A	19920416	CA 2028016	A	19901019	199227	B
US 5333194	A	19940726	US 90598244	A	19901015	199429	

Priority Applications (No Type Date): US 90598244 A 19901015
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes

CA 2028016 A 36 H04M-003/22
US 5333194 A 16 H04B-001/52
Abstract (Basic): CA 2028016 A

The autoequalising hybrid circuit provides a cancellation path to minimise the two-wire **receive** path signals that are reflected onto a two-wire **transmit** path from a **subscriber line interface circuit** . The hybrid circuit includes a variable impedance balance network. A tone generator injects a set of equalisation signals into the **receive** path which are used to control the setting, or equalisation, of the balance network. The tone generator also generates a supervisory signal into the **receive** path used to monitor the performance of the balance network. A detect circuit monitors the level of the reflected equalisation sidetone signals and produces balance signals whenever the equalisation signals fall to a null level. The detect circuit also monitors the supervisory sidetone signals and produces a recalibration signal whenever an abrupt change in the signals indicates that the balance network is no longer adequately cancelling their reflected signals.

A microprocessor controls the generation of the equalisation and supervisory signals and is connected to the detect circuit for monitoring production of the balance and the recalibration signals. When the hybrid is first activated, the microprocessor initially sets the balance network impedance with reference to the balance signals. After the balance network is equalised the microprocessor directs the tone generator to produce the supervisory sidetone signals. The microprocessor then monitors the **detect** circuit for recalibration **signals** and if they are produced, reequalises the impedance of the balance network.

USE - For automatically **adjusting** portion of **receive signal** feedback to **transmit** path to eliminate reflected side tone signal.

Dwg.1/3

Title Terms: AUTO; EQUAL; BIDIRECTIONAL; UNIDIRECTIONAL; HYBRID; NETWORK; TONE; GENERATOR; PRODUCE; SUPERVISION; SIGNAL; **RECEIVE** ; PATH; MONITOR; PERFORMANCE; BALANCE; NETWORK
Derwent Class: W01; W02
International Patent Class (Main): H04B-001/52; H04M-003/22
File Segment: EPI

20/5/17 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008497001 **Image available**
WPI Acc No: 1991-001085/199101
XRPX Acc No: N91-000880

Detector **of telephone charging** signals **- converts charging signals when private digital telephone system interfaces with analogue network**

Patent Assignee: ALCATEL BUSINESS SYSTEMS LTD (ALCA-N); ALCATEL BUSINESS SY (ALCA-N)
Inventor: BONVALLET A; CANONNE M; GIRARD R
Number of Countries: 013 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 404001	A	19901227	EP 90111424	A	19900618	199101	B
FR 2648655	A	19901221				199107	
US 5222129	A	19930622	US 90540435	A	19900619	199326	
EP 404001	B1	19940921	EP 90111424	A	19900618	199436	
DE 69012668	E	19941027	DE 612668	A	19900618	199442	
			EP 90111424	A	19900618		
ES 2062192	T3	19941216	EP 90111424	A	19900618	199505	

Priority Applications (No Type Date): FR 898118 A 19890619
Cited Patents: EP 279025; FR 2551604; GB 2005111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 404001	A				
Designated States (Regional): AT BE CH DE ES FR GB IT LI NL SE					
US 5222129	A		6	H04M-001/74	
EP 404001	B1	F	8	H04Q-001/50	
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI NL SE					
DE 69012668	E			H04Q-001/50	Based on patent EP 404001
ES 2062192	T3			H04Q-001/50	Based on patent EP 404001

Abstract (Basic): EP 404001 A

An entry filter (4) is centred on the frequency of the expected charging signals. A sampler (6) is connected to the output of the filter and to the output of a clock (7).

The clock provides a signal with a frequency close to that of the expected charging signals. The sampler (6) provides input to a low-pass filter (8) which in turn provides input to a level detector (9). This outputs a charging **signal** (TX) whenever it **detects** a **signal** from the low-pass filter higher than a predetermined threshold. (7pp Dwg.No.2/2)

Title Terms: DETECT; TELEPHONE; CHARGE; SIGNAL; CONVERT; CHARGE; SIGNAL; PRIVATE; DIGITAL; TELEPHONE; SYSTEM; INTERFACE; ANALOGUE; NETWORK
Index Terms/Additional Words: CALL; METER
Derwent Class: W01
International Patent Class (Main): H04M-001/74; H04Q-001/50
International Patent Class (Additional): H04M-015/28
File Segment: EPI

20/5/18 (Item 17 from file: 350)

008442240 **Image available**
WPI Acc No: 1990-329240/199044
XRPX Acc No: N90-252041

Telecommunications line interface circuit protection device - has brittle substrate which fractures due to overtemperature causing opening of thick film resistor and fuse conductor

Patent Assignee: GEC PLESSEY TELECOM LTD (ENGE); GEC PLESSEY TELECOM (ENGE); GPT LTD (ENGE)
Inventor: STIBILA M E
Number of Countries: 017 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 395231	A	19901031	EP 90303518	A	19900402	199044	B
GB 2230921	A	19901031	GB 899354	A	19890425	199044	
AU 9053689	A	19901101				199051	
CA 2014086	A	19901025				199103	
FI 9002057	A	19901026				199107	
JP 3074136	A	19910328	JP 90108556	A	19900424	199119	
CN 1046824	A	19901107				199129	
PT 93869	A	19911129				199201	
EP 395231	A3	19920205	EP 90303518	A	19900402	199323	
GB 2230921	B	19940105	GB 899354	A	19890425	199401	
EP 395231	B1	19951220	EP 90303518	A	19900402	199604	
DE 69024252	E	19960201	DE 624252	A	19900402	199610	
			EP 90303518	A	19900402		

Priority Applications (No Type Date): GB 899354 A 19890425
Cited Patents: NoSR.Pub; FR 2081828; FR 2246970; US 4494104; US 4562509
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 395231	A				
Designated States (Regional): BE DE ES FR GB IT LU NL SE					
GB 2230921	B		3	H04M-001/74	

EP 395231 B1 E 17 H01H-085/046
Designated States (Regional): BE DE DK ES FR GB GR IT LU NL SE
DE 69024252 E H01H-085/046 Based on patent EP 395231

Abstract (Basic): EP 395231 A
The device comprises a flat substrate of non-conductive, frangible material upon which a resistive component and a fuse conductor reside in an adjacent relationship on a common surface.
The resistive component is part of a first circuit, and the fuse conductor is part of a second circuit. The resistive component, at the time of an overcurrent, becomes hot and causes a heating of the near surface of the frangible substrate.
The frangible substrate, as a result of the uneven heating of its opposite surface, elongates and then fractures the fracturing of the frangible substrate bringing about a fracturing of the resistive component as well as a fracturing of the fuse conductor. This effects an interruption of the first circuit as well as a simultaneous interruption of the second circuit.
USE - For protecting a **subscriber line interface circuit**.
Dwg.g.1/10
Title Terms: TELECOMMUNICATION; LINE; INTERFACE; CIRCUIT; PROTECT; DEVICE; BRITTLE; SUBSTRATE; FRACTURE; OVERTEMPERATURE; CAUSE; OPEN; THICK; FILM; RESISTOR; FUSE; CONDUCTOR
Derwent Class: W01; X13
International Patent Class (Main): H01H-085/046; H04M-001/74
International Patent Class (Additional): H01C-007/12; H01H-085/00; H01H-085/04; H01H-085/048; H02H-003/08; H02H-005/04; H02H-009/00; H04M-003/18; H04M-019/08
File Segment: EPI

20/5/19 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008235903 **Image available**
WPI Acc No: 1990-122904/199016
XRPX Acc No: N90-095247
Telecommunications subscriber line interface - comprises amplified direct current component of ring **and** tip **line outputs with reference voltage to determine if** tip **is off-hook**
Patent Assignee: GEC PLESSEY TELECOM LTD (ENGE)
Inventor: STIBILA M E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4862495	A	19890829	US 88184860	A	19880422	199016	B

Priority Applications (No Type Date): US 88184860 A 19880422

Abstract (Basic): US 4862495 A
The telecommunications subscriber line interface includes a differential mode feedback circuit having a feed shut down control input, arranged to monitor a **ring** line and a **tip** line, and generate a current output which is applied to a converter to generate a voltage output, and a first amplifier arranged to monitor the **ring** and **tip** lines and generate an output which is proportional to a common-mode current flowing in the **ring** and **tip** lines when the **subscriber line interface circuit** is in a feed shut down mode as dictated by the output from differential mode feedback circuit.
A second amplifier is arranged to amplify a direct current component of the output from the first amplifier and attenuate the **alternating current** component of the output from the first amplifier. A comparator **receives** the amplified direct current component and compares it with a reference voltage to determine if the

tip party is off-hook.
USE/ADVANTAGE - 'Party line' multi-subscriber phones. Cost affective.
Dwg.1/11
Title Terms: TELECOMMUNICATION; SUBSCRIBER; LINE; INTERFACE; COMPRISE; AMPLIFY; DIRECT; CURRENT; COMPONENT; **RING** ; **TIP** ; LINE; OUTPUT; REFERENCE; VOLTAGE; DETERMINE; **TIP** ; HOOK
Derwent Class: W01
International Patent Class (Additional): H04M-015/36
File Segment: EPI

20/5/20 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008115265 **Image available**
WPI Acc No: 1990-002266/199001
XRPX Acc No: N90-001644
ISDN network termination unit - has identifier code holder and decision unit to establish data link on D-channel
Patent Assignee: NEC CORP (NIDE)
Inventor: FUJIWARA R
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2220325	A	19900104	GB 8913119	A	19890607	199001	B
AU 8936108	A	19891214				199005	
JP 1309495	A	19891213	JP 88138488	A	19880607	199005	
US 4999836	A	19910312	US 89362778	A	19890607	199113	
GB 2220325	B	19920819	GB 8913119	A	19890607	199234	
CA 1309195	C	19921020	CA 601864	A	19890606	199248	

Priority Applications (No Type Date): JP 88138488 A 19880607
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2220325	A		31		
GB 2220325	B			H04Q-011/04	
CA 1309195	C			H04Q-011/04	

Abstract (Basic): GB 2220325 A
The ISDN network termination unit connects a user's bus line (13) connected to terminal equipment and a subscriber line (10) extending from an exchange. It **receives** and **transmits** a D channel signal from one of the exchanges and each terminal equipment to the other. The D channel **signal** includes an **identifier** code field.
To establish a data link between the terminal equipments without use of the subscriber line and the exchange the network termination unit includes an identifier code holder (45) for holding a predetermined identifier code and a deciding circuit (37, 38, 47) for deciding whether or not the identifier code from a specific terminal equipment is equal to the predetermined identifier code. When both are equal, the D channel signal is **returned** by a **returning** circuit (48) to the terminal equipments through the user's line.
ADVANTAGE - Efficient use of D channel.
4/4
Title Terms: ISDN; NETWORK; TERMINATE; UNIT; IDENTIFY; CODE; HOLD; DECIDE; UNIT; ESTABLISH; DATA; LINK; CHANNEL
Derwent Class: W01
International Patent Class (Main): H04Q-011/04
International Patent Class (Additional): H04J-003/12; H04L-005/22; H04L-011/02; H04M-001/00; H04M-011/06; H04Q-005/00
File Segment: EPI

20/5/21 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008074563
WPI Acc No: 1989-339675/198946
XRPX Acc No: N89-258568
Subscriber line interface circuit **for telecommunication network - has loop** current detector **for providing output** signal **representing DC resistance in telecommunications** transmission **line**
Patent Assignee: SIEMENS CORP RES & SUPPORT (SIEI)
Inventor: SINBERG H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4866768	A	19890912				198946	B

Priority Applications (No Type Date): US 85749064 A 19850626; US 876317 A 19870114

Abstract (Basic): US 4866768 A
The telephone station **subscriber line interface circuit** comprises a loop **current sensing** circuit for providing an output signal proportionately representative of DC resistance in the telecommunications **transmission** line. A **ring** -side driving circuit is coupled to the loop **current sensing** circuit and is responsive to the output **signal** for providing an **alternating current voltage** source and a direct current voltage source to a **transmit** amplifier in periods of high constant DC resistance in the telecommunications **transmission** line.
The **ring** -side driving circuit maintains the output of the **alternating current voltage** source constant to the **transmit** amplifier and automatically transfers from a constant direct current voltage source to a constant direct current source in the event of a decrease in the DC resistance in the telecommunications **transmission** line **sensed** by the loop **current sensing** circuit. (8pp Dwg.No.2/5)
Title Terms: SUBSCRIBER; LINE; INTERFACE; CIRCUIT; TELECOMMUNICATION; NETWORK; LOOP; CURRENT; DETECT; OUTPUT; SIGNAL; REPRESENT; DC; RESISTANCE ; TELECOMMUNICATION; **TRANSMISSION** ; LINE
Index Terms/Additional Words: PABX
Derwent Class: W01
International Patent Class (Additional): H04M-019/00
File Segment: EPI

20/5/22 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008044160 **Image available**
WPI Acc No: 1989-309272/198942
XRPX Acc No: N89-235656
Automatic subscriber line interface in-circuit tester - has circuit to receive transmit , receive , **hook status, ringing and** ring **trip signals and compare with expected signal**
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: CHISM W R
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4860332	A	19890822	US 88221062	A	19880719	198942	B
EP 352040	A	19900124	EP 89307191	A	19890714	199004	
JP 2079655	A	19900320	JP 89187206	A	19890718	199017	
EP 352040	B1	19940420	EP 89307191	A	19890714	199416	
DE 68914738	E	19940526	DE 614738	A	19890714	199422	

EP 89307191 A 19890714

Priority Applications (No Type Date): US 88221062 A 19880719
Cited Patents: 2.Jnl.Ref; A3...9116; DE 3215680; DE 3500848
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4860332	A		15		
EP 352040	A				
	Designated States (Regional): DE FR GB				
EP 352040	B1	E	21	H04M-003/30	
	Designated States (Regional): DE FR GB				
DE 68914738	E			H04M-003/30	Based on patent EP 352040

Abstract (Basic): US 4860332 A

The automated apparatus is capable of testing the functioning of the **subscriber line interface circuit** ; by applying analog voltage to the **tip** and **ring** pins and recording the resulting **transmit** signals. One analog voltage signal is applied to the **receive** pin and the resulting signals are recorded on the **tip** and **ring** pins. Onhook and offhook signals are applied to the **tip** and **ring** pins and the resulting hook status signal is **received** . A **ring** command is applied to the **ring** control pin and the resulting **ring** signal is **received** . The offhook signal is applied to the **tip** and **ring** pins and the resulting **ring** trip signal is **received** . In conducting these tests, the automated apparatus electrically overdrives any analog or digital signal from associated components on the circuitry.

ADVANTAGE - High speed.

Dwg.2/7

Title Terms: AUTOMATIC; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; TEST; CIRCUIT ; **RECEIVE** ; **TRANSMIT** ; **RECEIVE** ; HOOK; STATUS; **RING** ; **RING** ; TRIP; SIGNAL; COMPARE; SIGNAL
Derwent Class: W01
International Patent Class (Main): H04M-003/30
International Patent Class (Additional): H04M-001/24; H04Q-003/42
File Segment: EPI

20/5/23 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007797524
WPI Acc No: 1989-062636/198909
XRPX Acc No: N89-047799

Concentrator system for emergency calls in congested traffic - uses permanently provided or cleared channel to complete call on subscriber dialling emergency destination address

Patent Assignee: NEC CORP (NIDE)
Inventor: SASAKI Y
Number of Countries: 007 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 304955	A	19890301	EP 88114048	A	19880829	198909	B
JP 1055926	A	19890302	JP 87213253	A	19870827	198915	
JP 1055930	A	19890302	JP 87213257	A	19870827	198915	
JP 1055931	A	19890302	JP 87213258	A	19870827	198915	
AU 8821632	A	19890302				198918	
US 4839892	A	19890613	US 88237204	A	19880829	198930	
CA 1299706	C	19920428	CA 575797	A	19880826	199222	
EP 304955	B1	19940112	EP 88114048	A	19880829	199403	
DE 3887034	G	19940224	DE 3887034	A	19880829	199409	
			EP 88114048	A	19880829		

Priority Applications (No Type Date): JP 87213258 A 19870827; JP 87213253 A

19870827; JP 87213257 A 19870827
Cited Patents: 3.Jnl.Ref; A3...9024; DE 3334886; EP 136517; JP 59089044; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 304955	A	E	23		
Designated States (Regional): DE GB IT					
US 4839892	A		21		
EP 304955	B1	E	31	H04Q-007/04	
Designated States (Regional): DE GB IT					
DE 3887034	G			H04Q-007/04	Based on patent EP 304955
CA 1299706	C			H04Q-007/04	

Abstract (Basic): EP 304955 A
Demand-assigned speech or data channels are constantly monitored by a central station to detect when they are congested. When an emergency call is **received** from a subscriber terminal, typically in the form of a 'hook flash' or momentary depression of the switch hook, a dial tone is sent to the terminal if the emergency call occurs simultaneously with the detection of the channel congestion.
On hearing the dial tone, the subscriber dials an emergency destination address which is **received** by a remote station, compared with a list of predetermined addresses and verified if it matches one of the predetermined addresses. The dialled information is sent from that remote station to the central station, where it is relayed to an access point of the switched telecommunication network. An emergency channel is then established between the subscriber terminal and the network for routing the emergency call.
ADVANTAGE - Allows emergency call from any subscriber to be completed when demand-assigned channels are congested with traffic
Title Terms: CONCENTRATE; SYSTEM; EMERGENCY; CALL; CONGESTED; TRAFFIC; PERMANENT; CLEAR; CHANNEL; COMPLETE; CALL; SUBSCRIBER; DIAL; EMERGENCY; DESTINATION; ADDRESS
Derwent Class: W01; W02
International Patent Class (Main): H04Q-007/04
International Patent Class (Additional): H04B-007/24; H04J-003/00; H04M-007/14
File Segment: EPI

20/5/24 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007691110 **Image available**
WPI Acc No: 1988-325042/198846
XRPX Acc No: N88-246289
Telephone subscriber line interface circuit **protection arrangement - has switching circuit which is opened in response to excessive** voltage **or** current detected **on line**
Patent Assignee: NORTHERN TELECOM LTD (NELE)
Inventor: ROSCH W; ROSENBAUM S D; ROSCH R W; ROSEMBAUM S D
Number of Countries: 011 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 291169	A	19881117	EP 88303286	A	19880413	198846	B
JP 63304793	A	19881213	JP 88116009	A	19880514	198904	
CA 1260171	A	19890926				198944	
CN 1030169	A	19890104				198949	
US 4947427	A	19900807	US 89423501	A	19891012	199034	N
EP 291169	B1	19921223	EP 88303286	A	19880413	199252	
DE 3876852	G	19930204	DE 3876852	A	19880413	199306	
			EP 88303286	A	19880413		
KR 9614224	B1	19961014	KR 885649	A	19880514	199928	

Priority Applications (No Type Date): CA 537286 A 19870515; US 89423501 A

19891012
Cited Patents: EP 209973; JP 60086995; US 4514595; WO 8602786; 1.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 291169	A	E	9		
Designated States (Regional): AT DE FR GB NL SE					
US 4947427	A		7		
EP 291169	B1	E	10	H04M-003/18	
Designated States (Regional): AT DE FR GB NL SE					
DE 3876852	G			H04M-003/18	Based on patent EP 291169
KR 9614224	B1			H04M-001/74	

Abstract (Basic): EP 291169 A

The subscriber line (10) is connected through an isolating relay (14) to a **current sensing** circuit (12). A **voltage sensing** circuit (18) is arranged to **sense voltage** on the line by way of series-opposed diodes (36) connected between the **tip** and **ring** wires (T,R).

A control circuit (16) connected both to the **voltage sensing** circuit and to the **current sensing** circuit is arranged to open the isolating relay in the event of either or both of excessive **voltage** and **current** being **sensed** on the line.

ADVANTAGE - Chattering is avoided and high ringing voltages are prevented.

2/2

Title Terms: TELEPHONE; SUBSCRIBER; LINE; INTERFACE; CIRCUIT; PROTECT; ARRANGE; SWITCH; CIRCUIT; OPEN; RESPOND; EXCESS; VOLTAGE; CURRENT; DETECT ; LINE
Derwent Class: W01
International Patent Class (Main): H04M-001/74; H04M-003/18
International Patent Class (Additional): H02H-003/06; H02H-003/087; H02H-003/38; H04M-001/00; H04M-007/00; H04Q-003/42
File Segment: EPI

20/5/25 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007579074 **Image available**
WPI Acc No: 1988-213006/198830
XRPX Acc No: N88-162391
Electro-thermal isolator or coupler e.g. for telephone system - transmits information across electrical isolation boundaries, with voice signals transmitted via capacitive coupling
Patent Assignee: HARRIS CORP (HARO)
Inventor: FALATER S L; SNOWDEN M A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4757528	A	19880712	US 86903785	A	19860905	198830	B

Priority Applications (No Type Date): US 86903785 A 19860905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4757528	A		11		

Abstract (Basic): US 4757528 A

The electro-thermal isolator coupler includes a pair of **electrically isolated** thermal **receivers** specifically spaced from an **electrically isolated** thermal **transmitter** such that their combined signals will produce a thermally compensated electrical output. A second pair of electrically thermal **receivers** is included in an error circuit which corrects the driver of the thermal **transmitter** for losses across the thermal coupler.S Depending upon the

use, the thermal coupler can be used in combination with RF capacitive coupling. Individual power terminals for the **electrically isolated** regions assure **electric isolation** .

USE/ADVANTAGE - For **subscriber line interface circuit** . Insensitive to ambient temp..

,8/13

Title Terms: ELECTRO; THERMAL; ISOLATE; COUPLE; TELEPHONE; SYSTEM; **TRANSMIT** ; INFORMATION; ELECTRIC; ISOLATE; BOUNDARY; VOICE; SIGNAL; **TRANSMIT** ; CAPACITANCE; COUPLE

Index Terms/Additional Words: **SUBSCRIB ER_LINE_** ; LINE; INTERFACE; CIRCUIT

Derwent Class: U11; U12; U13; W01

International Patent Class (Additional): H01L-031/00; H04M-007/00

File Segment: EPI

20/5/26 (Item 25 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007289064

WPI Acc No: 1987-286071/198741

XRPX Acc No: N87-214406

Multiple-access communications system for intra-office switching - has loop check circuit associated with remote station line interface circuit for applying loop check signal

Patent Assignee: NEC CORP (NIDE)

Inventor: FUJIWARA R

Number of Countries: 010 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 241228	A	19871014				198741	B
AU 8771107	A	19871008				198747	
JP 63045997	A	19880226				198814	
US 4756018	A	19880705				198829	
CA 1267960	A	19900417				199020	
KR 9007153	B	19900929				199151	
EP 241228	B1	19921021	EP 87302892	A	19870402	199243	
DE 3782265	G	19921126	DE 3782265	A	19870402	199249	
			EP 87302892	A	19870402		

Priority Applications (No Type Date): JP 8677540 A 19860405

Cited Patents: 2.Jnl.Ref; A3...8924; EP 120718; JP 60126997; No-SR.Pub; US 3778555; US 3917908; US 4284848

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 241228	A	E	29		
Designated States (Regional): DE FR GB NL SE					
US 4756018	A		14		
EP 241228	B1	E	15	H04Q-007/04	
Designated States (Regional): DE FR GB NL SE					
DE 3782265	G			H04Q-007/04	Based on patent EP 241228

Abstract (Basic): EP 241228 A

A central station is connected to a telecommunications switching system and to a remote station. Each station has a switching matrix. N central station line interfaces are connected to subscriber line terminals of the switching system and are terminated at the switching matrix. M (MCN) central station trunk circuits connected to **transmission** facilities are terminated at the matrix. A remote station controller (18) is associated with the remote-station subscriber line interfaces (15-1..15-n) and remote-station trunk circuits for establishing switched connections between them in the matrix.

The loop check circuit applies a loop check signal to one end of a connection t up between two of the remote-station line interfaces via the **transmission** facilities and switching system. A signal is

received from the detector of one of the remote station line interfaces connected to the other end of the connection for causing the controller to identify the line interfaces to cause the switching matrix to set up a connection between them and to clear the first connection.

USE - Multiple access radio telephone system

Title Terms: MULTIPLE; ACCESS; COMMUNICATE; SYSTEM; INTRA; OFFICE; SWITCH; LOOP; CHECK; CIRCUIT; ASSOCIATE; REMOTE; STATION; LINE; INTERFACE; CIRCUIT; APPLY; LOOP; CHECK; SIGNAL
Derwent Class: W01
International Patent Class (Main): H04Q-007/04
International Patent Class (Additional): H04B-007/00; H04M-007/14; H04Q-003/58
File Segment: EPI

20/5/27 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004020866
WPI Acc No: 1984-166408/198427
XRPX Acc No: N84-123857

Subscriber line interface circuit **for telephone system - has differential amplifier connected to two-wire line and two feedback loops to synthesise required impedance**

Patent Assignee: NEC CORP (NIDE)
Inventor: ARAI M; HAYASHI T; SHINOZUKA T
Number of Countries: 011 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 112731	A	19840704	EP 83307997	A	19831229	198427	B
AU 8322978	A	19840705				198434	
JP 59122110	A	19840714	JP 82229990	A	19821229	198434	
JP 59123307	A	19840717	JP 82229070	A	19821228	198434	
JP 59231930	A	19841226	JP 83106206	A	19830614	198507	
JP 60051359	A	19850322	JP 83159825	A	19830831	198518	
CA 1206649	A	19860624				198630	
US 4600811	A	19860715	US 83565975	A	19831227	198631	
EP 112731	B	19881109				198845	
DE 3378455	G	19881215				198851	

Priority Applications (No Type Date): JP 83215562 A 19831116; JP 82229070 A 19821228; JP 82229990 A 19821229; JP 83106206 A 19830614; JP 83159825 A 19830831
Cited Patents: 1.Jnl.Ref; A3...8626; FR 2485295; GB 2064269; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 112731	A	E	35		
Designated States (Regional): BE DE FR GB IT NL SE					
EP 112731	B	E			
Designated States (Regional): BE DE FR GB IT NL SE					

Abstract (Basic): EP 112731 A

The differential amplifier (1) is connected to a **tip** , **ring** terminal (T,R). The output terminals of the amplifier are connected through a first feedback loop (f1) to an input of a **tip** driver (2) and an input of a **ring** driver (3). The second feedback loop (f2) includes an AC feedback circuit (4) and a third feedback loop (f3) includes a DC feedback circuit (5).

The first feedback loop (f1) operates to increase the impedance values of resistances (RB) which are synthesised battery feed resistances. The C feedback loop provides a two-wire to four-wire conversion function. Since the second and third feedback loops are required to synthesise a required impedance over a given frequency

range, high precision is required only of the first feedback loop. This reduces the number of high precision components which are required.

1/9

Title Terms: SUBSCRIBER; LINE; INTERFACE; CIRCUIT; TELEPHONE; SYSTEM; DIFFERENTIAL; AMPLIFY; CONNECT; TWO-WIRE; LINE; TWO; FEEDBACK; LOOP; SYNTHESIS; REQUIRE; IMPEDANCE
Derwent Class: W01
International Patent Class (Additional): H04M-001/76; H04M-003/00; H04M-007/00; H04M-019/00; H04Q-003/00
File Segment: EPI

20/5/28 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003721085
WPI Acc No: 1983-717277/198329
XRPX Acc No: N83-127802

Digital loop transceiver for interfacing PABX to subscriber set - has A-D converter, and supports two channels whose digital data words and signalling information are time multiplexed together

Patent Assignee: MOTOROLA INC (MOTI)
Inventor: KELLY S H; WURZBURG H
Number of Countries: 008 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8302379	A	19830707				198329	B
EP 97166	A	19840104	EP 82903416	A	19821004	198402	
JP 59500037	W	19840105	JP 82503422	A	19821004	198407	
US 4432089	A	19840214	US 81334412	A	19811224	198409	
CA 1187969	A	19850528				198526	
EP 97166	B	19880127				198804	
DE 3278065	G	19880303				198810	

Priority Applications (No Type Date): US 81334412 A 19811224
Cited Patents: 1.Jnl.Ref; US 3924077; US 3978290; US 4145574; US 4281410; EP 36622; EP 50414; JP 56032847; US 3665328; US 4232293
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8302379	A	E	50		
Designated States (National): JP					
Designated States (Regional): DE FR GB NL SE					
EP 97166	A	E			
Designated States (Regional): DE FR GB NL SE					
EP 97166	B	E			
Designated States (Regional): DE FR GB NL SE					

Abstract (Basic): WO 8302379 A

The private automatic branch exchange (PABX) has a number of digital line cards for coupling two subscriber sets via subscriber lines. In each digital line card a digital loop transceiver (DLT) operates in a master mode to couple the digital data bus of the PABX to the subscriber line via a **subscriber line interface circuit** (38) in response to control signals provided by the PABX on the control bus.

In each subscriber set a DLT operates in a slave mode to couple the set to the subscriber line via a **subscriber line interface circuit** and to provide control signals required by the other components. Those DLT's provide communication on each of two channels with the digital data words on one channel being treated the same as those on the other channel. This system enables digital data words to be communicated at significantly higher speeds over the existing installed base of subscriber lines without any redesign or modification of the conventional digital PABX.

Title Terms: DIGITAL; LOOP; TRANSCEIVER; INTERFACE; PABX; SUBSCRIBER; SET; ANALOGUE-DIGITAL; CONVERTER; SUPPORT; TWO; CHANNEL; DIGITAL; DATA; WORD; SIGNAL; INFORMATION; TIME; MULTIPLEX
Index Terms/Additional Words: PRIVATE; AUTOMATIC; BRANCH; EXCHANGE
Derwent Class: W01
International Patent Class (Additional): H04J-003/00; H04L-011/00; H04M-003/42; H04M-009/00; H04Q-003/58; H04Q-005/20; H04Q-011/04
File Segment: EPI

20/5/29 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003365861
WPI Acc No: 1982-M3887E/198238
Loop differential detector for telephone network - detects **loop by logic** signal **provided when asymmetry is introduced into supply bridge for subscriber line equipment**
Patent Assignee: TRT TELECOM RADIOELEC TEL SA (TRTT)
Inventor: FORESTIER A
Number of Countries: 009 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 60006	A	19820915	EP 82200262	A	19820303	198238	B
FR 2501940	A	19820917				198244	
JP 57160296	A	19821002				198245	
US 4456791	A	19840626	US 82356604	A	19820309	198428	
EP 60006	B	19841121				198447	
DE 3261258	G	19850103				198502	

Priority Applications (No Type Date): FR 814850 A 19810311
Cited Patents: DE 2918270; EP 11720; EP 17763; FR 2324181; FR 2324183
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 60006	A	F	7		
Designated States (Regional): BE CH DE FR GB LI SE					
EP 60006	B	F			
Designated States (Regional): BE CH DE FR GB LI SE					

Abstract (Basic): EP 60006 A
The subscriber line wires (1,1') are connected to capacitively-coupled terminals (2,2') via half-windings (3,3') of a transformer whose other winding **transmits** speech currents to the exchange. These terminals are **returned** to the positive (earth) and negative central battery terminals (6,6') via two resistive branches, in one of which an additional resistor (8) is switched in or out (9) by a logic signal (F) from the exchange.
A differential detector (10) detects the loop by a logic signal (B1) when the additional resistor is shorted out and the bridge is symmetrical. A comparator (11) detects the loop by a logic logic signal (B2) when the bridge is asymmetrical. A low-pass filter (12) eliminates induced longitudinal currents at industrial frequency so that a logic circuit (13) ensures correct detection in either condition of the bridge
Title Terms: LOOP; DIFFERENTIAL; DETECT; TELEPHONE; NETWORK; DETECT; LOOP; LOGIC; SIGNAL; ASYMMETRIC; INTRODUCING; SUPPLY; BRIDGE; SUBSCRIBER; LINE; EQUIPMENT
Derwent Class: W01
International Patent Class (Additional): H04M-003/08; H04M-019/00; H04Q-003/00
File Segment: EPI

26/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009850625 **Image available**
WPI Acc No: 1994-130481/199416
XRPX Acc No: N95-210687
Semiconductor **integrated comparator circuit - has control signal input terminal for** receiving **control signal, and first input terminal and second input terminal coupled to input terminals**
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI DENKI KK (MITQ)
Inventor: ARAYA Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6077786	A	19940318	JP 92227279	A	19920826	199416	B
US 5440253	A	19950808	US 93105809	A	19930813	199537	

Priority Applications (No Type Date): JP 92227279 A 19920826
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6077786	A		13	H03K-005/08	
US 5440253	A		25	H03K-005/22	

Semiconductor **integrated comparator circuit**...

...**has control signal input terminal for** receiving **control signal, and first input terminal and second input terminal coupled to input terminals**

...Abstract (Basic): A **semiconductor integrated circuit** device comprises a...

...first input terminal and a second input terminal respectively connected to a first **transmission** line and to a second **transmission** line, and a comparison circuit formed on a **semiconductor** substrate. The comparison circuit comprises a control signal input terminal for **receiving** a control signal, a first input terminal and a second input terminal respectively coupled to the first and the second input terminals of the **semiconductor integrated circuit** device to **receive** potentials which are obtained in accordance with the first and second potentials which are inputted in to the first and the second input terminals of the **semiconductor integrated circuit** device, and an output terminal...

...of comparison under the control of the control signal. A control circuit formed on the **semiconductor** substrate comprises a control signal output terminal connected to the control signal input terminal of...

...a second input terminal respectively coupled to the first and second input terminals of the **semiconductor integrated circuit** device to **receive** potentials which are obtained in accordance with the first and the second potentials which are inputted to the first and the second input terminals of the **semiconductor integrated circuit** device, the control circuit outputting from its control signal output terminal a first control signal...

...USE/ADVANTAGE - For connection to first and second **transmission** lines for **receiving** dc voltages of first and second potentials from the first and second **transmission** lines, respectively, and signals which are superimposed on the dc voltages, the **semiconductor integrated circuit** device then performing **detection** regarding the dc **voltages**. Since the polarity **detection** circuit is highly densified, reduction is achieved in the number of parts which are necessary to fabricate the **semiconductor integrated circuit** device, and hence, in the size of the **semiconductor integrated circuit** device...

Title Terms: **SEMICONDUCTOR** ;
...International Patent Class (Additional): **H04M-019/00**

26/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003059592
WPI Acc No: 1981-F9628D/198126
Supply circuit for telephone subscriber's appts. or exchange circuit - compares current detected **on** ring **and** tip **lines to detect short-to-ground**
Patent Assignee: HITACHI LTD (HITA); NIPPON TEL & TELEG PUBL (NITE)
Inventor: HAGISHIMA K; KITANO J; TAKESHITA T
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2065420	A	19810624	GB 8038241	A	19801128	198126	B
FR 2471708	A	19810619				198132	
US 4385336	A	19830524				198323	
CA 1157597	A	19831122				198351	
GB 2065420	B	19840201				198405	

Priority Applications (No Type Date): JP 79156796 A 19791205

... **compares** current detected **on** ring **and** tip **lines to detect short-to-ground**
...Abstract (Basic): The current supplying circuit supplies a current to a terminal appts. through a **ring** line (1) and a **tip** line (2) which are connected through resistance elements (3, 4) to a potential source (6...

...respectively. The current supplying circuit includes a devices (8, 9) for generating first and second **detection signals** of amplitudes proportional to the currents flowing in the **ring** and **tip** lines, respectively...

...reference signal, and device (10) for comparing the signal difference between the first and second **detection signals** and the reference signal so as to produce a signal in accordance with the compared result. Thus a shorted-to-ground fault on the **ring** line or **tip** line is detected by monitoring (7) the signal produced in accordance with the compared result. After the shorted-to-ground fault is **detected** , the **current** supplying circuit is protected from breakdown. The circuit is suitable for being formed as a **semiconductor integrated circuit** .
...Title Terms: **RING** ;
...International Patent Class (Additional): **H04M-019/00**

34/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06238973 **Image available**
IDENTIFICATION DEVICE FOR CLOTHES

PUB. NO.: 11-180545 [JP 11180545 A]
PUBLISHED: July 06, 1999 (19990706)
INVENTOR(s): HASHIMOTO YUJI
APPLICANT(s): TEN TAC KK
APPL. NO.: 09-357113 [JP 97357113]
FILED: December 25, 1997 (19971225)
INTL CLASS: B65G-047/49; D03D-001/04; D06F-093/00; G06K-019/07; G06K-019/00; G09F-003/00

ABSTRACT

PROBLEM TO BE SOLVED: To provide an identification device capable of increasing an efficiency of a sorting operation when a large amount of clothes is handled by making it possible to automatically identify individual sheets and white garments.

SOLUTION: A data carrier 2 stored in a container 4 made of film and fixed to clothes is formed of a semiconductor device 12 and an antenna 11. The antenna 11 is print-wired on a flexible printed circuit board 10, and the data carrier 2 is provided with connection terminals to be connected electrically to the antenna 11, and forms an **integrated circuit** for outputting **identification signals** input beforehand to the antenna 11 in the **semiconductor** device 12 when the antenna 11 receives a transmission command signal.

34/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04368637 **Image available**
IC MEMORY CARD

PUB. NO.: 06-012537 [JP 6012537 A]
PUBLISHED: January 21, 1994 (19940121)
INVENTOR(s): TAKEMOTO SATORU
APPLICANT(s): FUJI PHOTO FILM CO LTD [000520] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-167167 [JP 92167167]
FILED: June 25, 1992 (19920625)
INTL CLASS: [5] G06K-019/07; G11C-005/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 30.1 (MISCELLANEOUS GOODS -- Office Supplies); 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)
JOURNAL: Section: P, Section No. 1727, Vol. 18, No. 214, Pg. 147, April 15, 1994 (19940415)

ABSTRACT

PURPOSE: To provide the IC memory card which can normally transmit and receive data to and from a host processor regardless of whether the source voltage supplied from the host processor is 5 or 3V.

CONSTITUTION: The source voltage supplied from the host processor is **detected** by a **voltage detecting** circuit 202 in the **IC memory card** and its information 308 is supplied to a timing control circuit 204.

The timing control circuit 204 switches the access times of memory elements 201a and 201b for 5V driving to short pulse width when the detected voltage is 5V or to long pulse width when 3V. When the information is received, a read/write control circuit 203 receives pulse width information 311 from the timing control circuit 204 and supplies write data 304 to the memory elements 201a and 201b in a short time at the time of 5V or in a long time at the time of 3V. At the time of 3V, a wait test signal 310 is sent out to the host processor to match the timing.

34/5/3 (Item 3 from file: 347)

02750038 **Image available**
ELECTRIC PARTS CONTROLLER FOR VEHICLE

PUB. NO.: 01-047638 [JP 1047638 A]
PUBLISHED: February 22, 1989 (19890222)
INVENTOR(s): INOMATA TERUHISA
HASHIMOTO TAKERU
APPLICANT(s): MITSUBISHI CABLE IND LTD [000326] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-203325 [JP 87203325]
FILED: August 14, 1987 (19870814)
INTL CLASS: [4] B60R-016/02; H04Q-009/00
JAPIO CLASS: 26.2 (TRANSPORTATION -- Motor Vehicles); 22.3 (MACHINERY -- Control & Regulation)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)
JOURNAL: Section: M, Section No. 833, Vol. 13, No. 237, Pg. 13, June 05, 1989 (19890605)

ABSTRACT

PURPOSE: To reduce containing space for electric parts and to enable compensation of defective portion upon occurrence of trouble by forming respective control units such as wiper control section on a single IC board and controlling respective electric parts through a multiplex transmission cable.

CONSTITUTION: Control signals for electric parts 4 are fed to a signal processor IC6 corresponding to signals fed from various switches then multiplexed through a multiplex transmitting/receiving section 20 and transmitted through a transmission cable 9 to a multiplex transmitting/receiving section 22 at the side of a driving module 8. The electric parts 4 are driven through a power converting section 24 based on the signals **received** at the multiplex **transmitting / receiving** section 22. Output **signals** from **sensors** provided for the **electric** parts 4 are **transmitted** through the multiplex **transmitting / receiving** section 22 to the side of IC6. Upon trouble of the electric parts 4, signals are fed from the sensors to a trouble compensating section 16 and optional operation control signals can be outputted in response to the sensor signals.

34/5/4 (Item 4 from file: 347)

02432096 **Image available**
ELECTRIC SIGNAL REPEATER

PUB. NO.: 63-048996 [JP 63048996 A]
PUBLISHED: March 01, 1988 (19880301)
INVENTOR(s): FUKUI KENSUKE

APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-193459 [JP 86193459]
FILED: August 18, 1986 (19860818)
INTL CLASS: [4] H04Q-009/00; H04B-003/54
JAPIO CLASS: 22.3 (MACHINERY -- Control & Regulation); 44.2 (COMMUNICATION -- Transmission Systems)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)
JOURNAL: Section: E, Section No. 637, Vol. 12, No. 265, Pg. 149, July 23, 1988 (19880723)

ABSTRACT

PURPOSE: To simplify the constitution of a memory circuit and to obtain the correct output of a good waveform by storing a signal converted into a parallel signal by a remote control IC in a memory and reading it as a serial signal by the use of a bidirectional terminal.

CONSTITUTION: Plural repeaters 2a-2n are connected to the housing information disk 1 of a home security system by a power line 3 and abnormality **detection signals** from various types of sensors 4a-4d are **received** through **transmitters** 5a-5d by the repeaters 2a-2n. The respective abnormal signals are received in the receiving circuit 7 of the repeaters 2a-2n and an input signal is converted from serial to parallel or parallel to serial by an IC8 for a remote control. To this IC8, an oscillator circuit 9 for supplying a clock pulse, a recording circuit 10 for temporarily recording a parallel signal from the IC8 and returning the signal in the IC again and an address switch circuit 11 for setting an address in the IC8 are connected and the serial signal is outputted to the power line 3 by a power carrying circuit 12.

34/5/5 (Item 5 from file: 347)

02146479 **Image available**
PORTABLE DATA COLLECTING DEVICE

PUB. NO.: 62-063379 [JP 62063379 A]
PUBLISHED: March 20, 1987 (19870320)
INVENTOR(s): FUKUSHIMA TOSHITAKA
SAKAMI YASUO
IZAKI SHOZO
WATANABE HIROYUKI
OKINA SHIGETAKA
TSUBOUCHI JUNICHI
ISHIZAKI MASAO
APPLICANT(s): SEIKO INSTR & ELECTRONICS LTD [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-202777 [JP 85202777]
FILED: September 13, 1985 (19850913)
INTL CLASS: [4] G06F-015/74; G06F-001/00; G06F-001/04
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.9 (INFORMATION PROCESSING -- Other)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS
JOURNAL: Section: P, Section No. 608, Vol. 11, No. 260, Pg. 11, August 22, 1987 (19870822)

ABSTRACT

PURPOSE: To obtain a portable data collecting device which is easy to be used, light, small-sized and can be used for a long period by one battery exchange by comprising a device with a CPU, a ROM, a RAM, a display part,

an input key, a battery **voltage detecting** circuit, an **electric power** source circuit, a **transmitting / receiving** coil and an interface LSI.

CONSTITUTION: By loading a program to a RAM 16, the program can be changed to a suitable program in accordance with a purpose. Since the communication with the external part is of an electronic magnetic induction system, the device is optimum as the portable data collecting device. By making a peripheral IC into one chip with CMOSIC, the power consumption is decreased. By driving with the constant voltage of 3.5V reduction and stopping the oscillation of a CPU except for the necessity, the average consumption electric current is minimized very much. By using the tuning fork type crystal resonator for an interface LSI 17, the device can be easily connected to the general personal computer, etc

34/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02058859 **Image available**
TRIMMING METHOD FOR SEMICONDUCTOR DEVICE

PUB. NO.: 61-272959 [JP 61272959 A]
PUBLISHED: December 03, 1986 (19861203)
INVENTOR(s): ODAJIMA MINORU
YAMAGATA MICHIAKI
ANDO YUKIKIYO
APPLICANT(s): YOKOGAWA ELECTRIC CORP [000650] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-114872 [JP 85114872]
FILED: May 28, 1985 (19850528)
INTL CLASS: [4] H01L-027/01; H01L-027/04
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JOURNAL: Section: E, Section No. 501, Vol. 11, No. 127, Pg. 106, April 21, 1987 (19870421)

ABSTRACT

PURPOSE: To improve yield by referring to an output from a temperature sensor unified with one part of a semiconductor wafer and trimming a semiconductor chip.

CONSTITUTION: A probe card 9 supplies temperature sensor IC chips 5 and reference-temperature sensors 6 formed to a wafer 2 with a power supply from a measurement system 10 while **transmitting** or **receiving signals** among both the **sensor IC** chips 5 and the sensors 6 and the measurement system 10. The operation of the measurement of the measurement system 10 is controlled by a CPU11. The CPU11 drives a laser 12 and an XY movable mirror 13 according to a predetermined algorithm corresponding to the results of measurement acquired by the measurement system 10, and executes trimming operation by laser beams.

34/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01790879 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 61-004979 [JP 61004979 A]
PUBLISHED: January 10, 1986 (19860110)
INVENTOR(s): MIZUKAMI MASAO
SUZUKI TORU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)

HITACHI MICRO COMPUT ENG LTD [470864] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-125232 [JP 84125232]
FILED: June 20, 1984 (19840620)
INTL CLASS: [4] G01R-031/28; G06F-011/22; H01L-021/82; H01L-027/10
JAPIO CLASS: 46.1 (INSTRUMENTATION -- Measurement); 42.2 (ELECTRONICS -- Solid State Components); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)
JOURNAL: Section: P, Section No. 462, Vol. 10, No. 152, Pg. 57, June 03, 1986 (19860603)

ABSTRACT

PURPOSE: To simplify circuit constitution by providing each flip-flop circuit with a diagnosing circuit composed of two kinds of transmission gates, and cascading a diagnosing circuit and an information holding circuit between flip-flop circuits, and thus constituting a shift register.

CONSTITUTION: Each flip-flop circuit of an information processing circuit is provided with a diagnosing circuit consisting of a latch circuit composed of a P- channel type **transmission** gate MOSFETQ23 which **receives** a **diagnostic** clock **signal** -.phi.S, N-channel type transmission gate MOSFETQ22, inverter circuit IV25, and feedback inverter circuit IV24. Then, respective flip-flop circuits are cascaded across a diagnostic circuit to constituted the shift register. Thus, elements signals are reduced in number to simplify the circuit constitution.

34/5/8 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015009495 **Image available**
WPI Acc No: 2003-070012/200307
XRPX Acc No: N03-054335

Audio device e.g. vehicle-mounted audio device has heat protective circuit to control power supply to each power supply circuit, based on temperature of semiconductor element in power amplification circuit

Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002247680	A	20020830	JP 200146050	A	20010222	200307	B

Priority Applications (No Type Date): JP 200146050 A 20010222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002247680	A		7	H04R-003/00	

Abstract (Basic): JP 2002247680 A

NOVELTY - The audio device has power amplification circuits (ch1-ch4) to amplify audio signal received from prescribed source and transmit it to speakers (SP1-SP4). The temperature of a **semiconductor** element in a **power** amplification circuit is **detected** . Based on the detection result, the power supply to each power supply is controlled stepwise according to priority, by a heat protective circuit (15).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for power amplification integrated circuit.

USE - E.g. vehicle-mounted audio device.

ADVANTAGE - Based on the temperature value of semiconductor, the power supply to each power supply circuit is controlled by heat protective circuit, thereby even when it mounts on high output circuit with high density, degradation of versatility is prevented effectively by heat protection.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of

the audio device. (Drawing includes non-English language text).
Heat protective circuit (15)
Power amplification circuits (ch1-ch4)
Speakers (SP1-SP4)
pp; 7 DwgNo 1/8
Title Terms: AUDIO; DEVICE; VEHICLE; MOUNT; AUDIO; DEVICE; HEAT; PROTECT; CIRCUIT; CONTROL; POWER; SUPPLY; POWER; SUPPLY; CIRCUIT; BASED; TEMPERATURE; SEMICONDUCTOR; ELEMENT; POWER; AMPLIFY; CIRCUIT
Derwent Class: U13; U24
International Patent Class (Main): H04R-003/00
International Patent Class (Additional): H01L-021/822; H01L-027/04; H03F-001/52; H05K-007/20
File Segment: EPI

34/5/9 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014521541 **Image available**
WPI Acc No: 2002-342244/200238
XRPX Acc No: N02-269122
Integrated device for electromagnetic protection, comprises insulator layers embedded in substrate below superimposed strip conductors on both sides of electric or electronic elements
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG); DE LA TORRE A (DTOR-I); GAMAND P (GAMA-I)
Inventor: DE LA TORRE A; GAMAND P
Number of Countries: 030 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1187206	A1	20020313	EP 2001203251	A	20010828	200238	B
JP 2002093810	A	20020329	JP 2001268493	A	20010905	200238	
US 20020074605	A1	20020620	US 2001946715	A	20010905	200244	
CN 1341964	A	20020327	CN 2001135759	A	20010901	200247	
KR 2002019413	A	20020312	KR 200154182	A	20010904	200262	

Priority Applications (No Type Date): FR 200011307 A 20000905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1187206	A1	F	13	H01L-023/552	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
JP 2002093810	A		8	H01L-021/3205	
US 20020074605	A1			H01L-031/119	
CN 1341964	A			H01L-023/58	
KR 2002019413	A			H01L-021/76	

Abstract (Basic): EP 1187206 A1
NOVELTY - The device for insulating electric or electronic elements (16,58) such as interconnection integrated on a semiconductor substrate (12), comprises insulator layers (84,86,90) embedded in the substrate and a set of superimposed strip conductors (60,62,64;66,68,70), in particular three on each side of the elements and extending along them. The height of the set is greater than that of the elements. The insulator layers (84,86) fill trenches (80,82) extending in the substrate perpendicular to its surface and along the elements (16,58) on each side and separating them from another element (18).
DETAILED DESCRIPTION - The superimposed strip conductors are electrically connected by feedthroughs (74,78;76,79). Each feedthrough extends to one or the other extremity of the strip conductors, or several mutually spaced feedthroughs connect the superimposed strip conductors. An electrically conducting layer (91) extends above the elements and connects the top-layer strip conductors (64,70). In a variant of the device, the semiconductor layer embedded in the

substrate below the element is of conductivity type opposite to that of the substrate so as to form a p-n junction with the substrate. In a variant of the device, several parallel trenches are transversal to the element, and each trench is filled with an insulator layer. In a variant of the device, a supplementary insulator layer extends in the substrate below the element and insulates a portion of the substrate where the element is formed from the rest of the substrate. In a variant of the device, an electric conductor and an electrically insulating layer where the conductor is formed are isolated by two parallel conductor layers comprising the insulating layer, and crossings connect the two conductor layers. In a variant of the device, the element is a waveguide demarcated by two parallel conductor layers and two crossings.

USE - In devices for electromagnetic protection, that is space insulation of an electric or electronic element integrated with a **semiconductor** substrate; for **isolating electric signals** propagating in connecting elements formed on a **semiconductor** substrate, which could perturb the functioning of other devices, such as a voltage-controlled oscillator; in devices such as transmitter-receiver integrated circuits where signals of different frequencies and types are used, e.g. analogue and digital; in millimeter wavelength and super-high frequency range.

ADVANTAGE - The device provides an efficient insulation of electric connections where signals propagate which can perturb the normal functioning of device, e.g. a clock signal which could interfere with analogue signals.

DESCRIPTION OF DRAWING(S) - The drawing is a partial perspective view of the device.

Substrate (12)
Insulator layer (14)
Electric or electronic elements (16,18,58)
Superimposed strip conductors (60,62,64,66,68,70)
Feedthrough (74,76,78,79)
Silica layer (77)
Trenches (80,82)
Insulator layers (84,86)
Conductor layer (91)
pp; 13 DwgNo 6/12

Title Terms: INTEGRATE; DEVICE; ELECTROMAGNET; PROTECT; COMPRISE; INSULATE; LAYER; EMBED; SUBSTRATE; BELOW; SUPERIMPOSED; STRIP; CONDUCTOR; SIDE; ELECTRIC; ELECTRONIC; ELEMENT
Derwent Class: U11; V04; W02
International Patent Class (Main): H01L-021/3205; H01L-021/76; H01L-023/552; H01L-023/58; H01L-031/119
International Patent Class (Additional): H01L-029/76; H01L-029/94; H01L-031/113; H01L-031/62; H05K-009/00
File Segment: EPI

34/5/10 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014180969 **Image available**
WPI Acc No: 2002-001666/200201
XRPX Acc No: N02-001182

Device manufacturing apparatus e.g. for semiconductor device, liquid crystal display, includes controller to determine manipulated variable of actuators based on signal from sensors

Patent Assignee: CANON KK (CANO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000349015	A	20001215	JP 99159145	A	19990607	200201	B

Priority Applications (No Type Date): JP 99159145 A 19990607
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 2000349015 A 11 H01L-021/027

Abstract (Basic): JP 2000349015 A
NOVELTY - A signal preprocessor (43) converts analog **detecting signals** from various **sensors** **detecting** controlled variables, into digital packets and **transmits** it. A controller **receives** the packet and determines the manipulated variable of actuators operating some system to be controlled.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the device manufacturing method.
USE - In e.g. exposure system, semiconductor manufacturing apparatus for manufacturing IC, LSI, LCD, image pick-up device of CCD, magnetic head.
ADVANTAGE - Reduces calculation load of controller. The devices are manufactured with high precision.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the signal preprocessor of exposure system.
Signal preprocessor (43)
pp; 11 DwgNo 1/13
Title Terms: DEVICE; MANUFACTURE; APPARATUS; SEMICONDUCTOR; DEVICE; LIQUID; CRYSTAL; DISPLAY; CONTROL; DETERMINE; MANIPULATE; VARIABLE; ACTUATE; BASED; SIGNAL; SENSE
Derwent Class: P84; Q63; T03; T06; U11; U14; W01; W04; W05
International Patent Class (Main): H01L-021/027
International Patent Class (Additional): F16F-015/02; G03F-007/20; G05B-015/02; H04L-012/28
File Segment: EPI; EngPI

34/5/11 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012388074 **Image available**
WPI Acc No: 1999-194181/199917
XRPX Acc No: N99-142472
Contact state detection mechanism of jig for connecting IC and IC test device - includes detector which detects condition when switch is not pressed to terminal, and sends signal to receiver of IC test device
Patent Assignee: NIPPON DENKI ENG KK (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 11038081 A 19990212 JP 97198774 A 19970724 199917 B

Priority Applications (No Type Date): JP 97198774 A 19970724
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 11038081 A 4 G01R-031/26

Abstract (Basic): JP 11038081 A
NOVELTY - When a pogo-pin (53) of an IC test device (51) breaks, a switch (15) of the jig is not pressed to a terminal (16), this condition is detected with the detector (13). The **detector** **sends** the **detection signal** to a **receiver** (54) in **IC** test device (51) through a **detection signal** terminal (14), indicating non-contact state of jig and **IC** test device.
USE - For jig used for connecting IC and IC test device.
ADVANTAGE - Prevents collection of wrong data. Informs abnormal contact condition of IC test device and jig for semiconductor test to operator. DESCRIPTION OF DRAWING(S) - The figure shows the expanded view of detection part during non-contact state of jig and **IC** test

device. (13) **Detector** ; (14) **Detection signal** terminal; (15) Switch; (16) Terminal; (51) **IC** test device; (53) Pogo- pin; (54) Receiver.

Dwg.2/3

Title Terms: CONTACT; STATE; DETECT; MECHANISM; JIG; CONNECT; IC; IC; TEST; DEVICE; DETECT; DETECT; CONDITION; SWITCH; PRESS; TERMINAL; SEND; SIGNAL; RECEIVE; IC; TEST; DEVICE
Derwent Class: S01; U11
International Patent Class (Main): G01R-031/26
International Patent Class (Additional): G01R-031/28; H01L-021/66
File Segment: EPI

34/5/12 (Item 5 from file: 350)

012249765 **Image available**
WPI Acc No: 1999-055872/199905
XRPX Acc No: N99-042398

Chargeable non-contact IC card processing system used in OA, FA, security system - has identification unit that generates AC magnetic field energy by which chargeable battery of IC card is charged

Patent Assignee: TOPPAN PRINTING CO LTD (TOPP)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10307898	A	19981117	JP 97119384	A	19970509	199905	B

Priority Applications (No Type Date): JP 97119384 A 19970509
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10307898	A		7	G06K-017/00	

Abstract (Basic): JP 10307898 A

The system has an identification unit (2) to generate AC magnetic field energy of specific frequency. The AC magnetic field is detected by a non-contact IC card (1). A receiver (6) of the IC card converts the received signal to specific data that is processed by a microprocessor (7).

The battery is charged using the AC magnetic field energy generated by the **identification** unit. Then, **power** is supplied from a chargeable battery (9) to the **receiver** , a **transmitter** (8) and the microprocessor.

USE - For traffic management, automatic ticket inspection machine.

ADVANTAGE - Avoids need for connection terminal in IC card for charging. Reduces damage of semiconductor portion in IC card by high voltage discharge.

Dwg.1/4

Title Terms: CHARGE; NON; CONTACT; IC; CARD; PROCESS; SYSTEM; OA; SECURE; SYSTEM; IDENTIFY; UNIT; GENERATE; AC; MAGNETIC; FIELD; ENERGY; CHARGE; BATTERY; IC; CARD; CHARGE
Derwent Class: T04; X16
International Patent Class (Main): G06K-017/00
International Patent Class (Additional): G06K-019/07
File Segment: EPI

34/5/13 (Item 6 from file: 350)

012181509 **Image available**
WPI Acc No: 1998-598422/199851
XRPX Acc No: N98-465827

Multi-wiring inspection apparatus for semiconductor testing device - has adaptor to receive current from voltage-current generator via electronic dummy pin unit and to supply received current to specific point of specific pattern substrate

Patent Assignee: ADVANTEST KK (ADVA-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10267980	A	19981009	JP 9771386	A	19970325	199851	B

Priority Applications (No Type Date): JP 9771386 A 19970325
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10267980	A		7	G01R-031/02	

Abstract (Basic): JP 10267980 A

The apparatus has a programmable voltage-current generator (12) to output arbitrary voltages or currents to an electronic dummy pin unit (38) based on the control signal from a test processor (2). A digital multimeter (13) measures the output current of the voltage-current generator and the voltage in a load resistor (R). A test head controller (36) regulates the operation of the switches of the electronic dummy pin unit sequentially based on the control signal from the test processor. The current from the voltage-current generator is sequentially switched to multiple points of an adaptor (40) via the electronic dummy pin unit based on the switching control signal from the test head controller.

The **adaptor transmits** the **received current** to a specific point of a specific pattern substrate (5). A connector (7) has a specific pin which receives current from the specific point of the specific pattern substrate via a wiring circuit (6). The relay of a wiring inspection board (14) is connected to each pin of the connector via a connection board (8) and a connection cable (9). The wiring inspection board supplies the current received via the connection cable to the load resistor.

USE - For testing semiconductor IC.

ADVANTAGE - Enables to inspect wiring even for large number of channels in multiple wiring circuit. Examines wiring circuit at high speed.

Dwg.1/3

Title Terms: MULTI; WIRE; INSPECT; APPARATUS; SEMICONDUCTOR; TEST; DEVICE; ADAPT; RECEIVE; CURRENT; VOLTAGE; CURRENT; GENERATOR; ELECTRONIC; DUMMY; PIN; UNIT; SUPPLY; RECEIVE; CURRENT; SPECIFIC; POINT; SPECIFIC; PATTERN; SUBSTRATE
Derwent Class: S01
International Patent Class (Main): G01R-031/02
File Segment: EPI

34/5/14 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012019939 **Image available**
WPI Acc No: 1998-436849/199837
Related WPI Acc No: 1994-000859; 1994-217039; 1994-366420; 1995-319977; 1996-170610; 1996-171157; 1996-505571; 1997-042559; 1997-271484; 1997-363815; 1998-158924; 1998-397890; 1998-412940; 1999-034418; 2000-222172; 2000-386256; 2001-030748; 2001-450893; 2001-578372; 2002-517213
XRPX Acc No: N98-340390

Hybrid or monolithic IC device with provision for remote identification for tracking inventories of ICs, locating and identifying stolen ICs - has transmitter in RF identification circuit, that transmits RF signal including identification number stored in memory after receiver receives

RF interrogation signal

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: TUTTLE J R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5787174	A	19980728	US 92899777	A	19920617	199837	B
			US 92990915	A	19921215		
			US 92990918	A	19921215		
			US 93168909	A	19931217		
			US 94263210	A	19940621		
			US 95422007	A	19950411		
			US 95489185	A	19950609		
			US 95556818	A	19951102		

Priority Applications (No Type Date): US 95556818 A 19951102; US 92899777 A 19920617; US 92990915 A 19921215; US 92990918 A 19921215; US 93168909 A 19931217; US 94263210 A 19940621; US 95422007 A 19950411; US 95489185 A 19950609
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5787174	A		10	H04L-009/32	CIP of application US 92899777
					CIP of application US 92990915
					Cont of application US 92990918
					CIP of application US 93168909
					CIP of application US 94263210
					CIP of application US 95422007
					CIP of application US 95489185
					Cont of patent US 5365551
					CIP of patent US 5497140
					CIP of patent US 5550650
					CIP of patent US 5572226
					CIP of patent US 5583850

Abstract (Basic): US 5787174 A

The device includes an IC package mounted with a main integrated circuit (1) such as microprocessor and an RF identification circuit (2). The RF identification circuit includes an ID number memory (3) for storing an identification number and an RF transceiver (4).

The RF transceiver includes a receiver (50) for **receiving** RF signals. A **transmitter** (52) of the RF transceiver transmits an **identification** RF **signal** including the stored **identification** number after the receiver receives an RF interrogation signal.

ADVANTAGE - Enables reliable monitoring of inventories of ICs by semiconductor manufacturers and distributors. Obstructs changing of ID number without destruction of IC.

Dwg.3/4

Title Terms: HYBRID; MONOLITHIC; IC; DEVICE; PROVISION; REMOTE; IDENTIFY; TRACK; INVENTORY; LOCATE; IDENTIFY; STOLEN; TRANSMIT; RF; IDENTIFY; CIRCUIT; TRANSMIT; RF; SIGNAL; IDENTIFY; NUMBER; STORAGE; MEMORY; AFTER; RECEIVE; RECEIVE; RF; INTERROGATION; SIGNAL
Derwent Class: W01
International Patent Class (Main): H04L-009/32
International Patent Class (Additional): H04L-009/32
File Segment: EPI

34/5/15 (Item 8 from file: 350)

010937127 **Image available**
WPI Acc No: 1996-434077/199643
Related WPI Acc No: 1996-434076
XRPX Acc No: N96-365687

Transponder for electronic identification security system - uses CMOS chip with embedded antennae which receive **and** transmit **signal to interrogator and a modulated** signal **is decoded to** identify **the transponder**

Patent Assignee: BRITISH TECHNOLOGY GROUP INTER-CORP (BRTE-N)
Inventor: SCHEELEN J

Number of Countries: 071 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9628880	A2	19960919	WO 96GB622	A	19960315	199643	B
AU 9650121	A	19961002	AU 9650121	A	19960315	199703	
WO 9628880	A3	19961212	WO 96GB622	A	19960315	199712	
EP 815638	A1	19980107	EP 96906870	A	19960315	199806	
			WO 96GB622	A	19960315		
JP 11502072	W	19990216	JP 96527396	A	19960315	199917	
			WO 96GB622	A	19960315		
KR 98702934	A	19980905	WO 96GB622	A	19960315	199938	
			KR 97706342	A	19970911		

Priority Applications (No Type Date): GB 955350 A 19950316
Cited Patents: Jnl.Ref; EP 281142; EP 336432; EP 367981; EP 377257; EP 513910; EP 590303; FR 2520950; FR 2636188; GB 2261973; JP 63064572; US 4380083; US 4773085; US 4876699; WO 8604705; WO 9113499; WO 9117515; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9628880	A2	E	41	H02M-007/219	
Designated States (National): AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN					
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG					
AU 9650121	A			H02M-007/219	Based on patent WO 9628880
EP 815638	A1	E		H02M-007/219	Based on patent WO 9628880
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 11502072	W		49	H04B-001/59	Based on patent WO 9628880
KR 98702934	A			H02M-007/219	Based on patent WO 9628880
WO 9628880	A3			H02M-007/219	

Abstract (Basic): WO 9628880 A

The passive transponder for an identification system comprises a single CMOS chip and uses a power antenna (18), and a rectifier circuit (26) to extract power from radiation impinging on the transponder and supplies the power to a storage capacitor (24). A data receive antenna (20) and a circuit (28) extract data from the received signal. The transponder also has a transmit antenna (22) and an EPROM stores data and supplies a signal to the transmit antenna which identifies the transponder. The three antenna coils are all provided in the form of embedded coils on a CMOS chip and may form a coil surrounding the core of the respective part of the IC, or may consist of a coil deposited on top of the passivation layer of the CMOS.

ADVANTAGE - Alignment of transponder with receptor coils is not necessary, can operate at a substantial distance

Dwg.2/14

Title Terms: TRANSPONDER; ELECTRONIC; IDENTIFY; SECURE; SYSTEM; CMOS; CHIP; EMBED; ANTENNA; RECEIVE; TRANSMIT; SIGNAL; INTERROGATION; MODULATE; SIGNAL; DECODE; IDENTIFY; TRANSPONDER
Derwent Class: T05; U24; W02; W05; W06
International Patent Class (Main): H02M-007/219; H04B-001/59
International Patent Class (Additional): G01R-019/175; G06K-019/07; G06K-019/077; H03K-005/13; H03K-017/082
File Segment: EPI

34/5/16 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009871690 **Image available**
WPI Acc No: 1994-151603/199418
XRPX Acc No: N94-139274
NMOS integrated circuit **esp. with** electrical isolation **between adjacent transistors - uses forward biased diode voltage drop to generate back bias, with diode connected between ground body and NMOS transistor surfaces**
Patent Assignee: SMC STANDARD MICROSYSTEMS CORP (SMCS-N)
Inventor: WANLASS F
Number of Countries: 019 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9409515	A1	19940428	WO 93US8652	A	19930914	199418	B
EP 616725	A1	19940928	EP 93921555	A	19930914	199437	
			WO 93US8652	A	19930914		
JP 7502382	W	19950309	WO 93US8652	A	19930914	199518	
			JP 94509998	A	19930914		
US 5422507	A	19950606	US 92961433	A	19921015	199528	
			US 94361175	A	19941221		
EP 616725	A4	19950329	EP 93921555	A	19930000	199612	

Priority Applications (No Type Date): US 92961433 A 19921015; US 94361175 A 19941221
Cited Patents: US 3865654; US 4476476; US 4647956; 1.Jnl.Ref; EP 84000
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9409515	A1	E	31	H01L-027/02	
Designated States (National): CA JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
EP 616725	A1	E	2	H01L-027/02	Based on patent WO 9409515
Designated States (Regional): DE FR GB IT					
JP 7502382	W		12	H01L-027/04	Based on patent WO 9409515
US 5422507	A		14	H01L-027/02	Cont of application US 92961433
EP 616725	A4			H01L-027/02	

Abstract (Basic): WO 9409515 A
The IC includes an internal circuit, and input/output circuitry which receives and sends electrical signals and receives power supply and reference voltages onto the chip. The internal circuit includes a diode with cathode connected to the reference voltage and anode coupled to the internal circuit NMOS transistor' sources, otherwise coupled to the reference voltage pref. ground. Application of a power supply and ground voltages to the Ic allows the internal circuit to perate between the power supply voltage and another voltage e.g a diode forward voltage drop above the reference voltage.
The diode may be a PN diode. The internal circuit NMOS transistors are pref. formed in p-wells, each coupled to the reference voltage, so that the NMOS transistor body connections are coupled directly to the ground voltage reference. The internal circuit PMOS transistors may have their sources coupled to the cathode of a second diode, with anode connected to the power supply voltage.
USE/ADVANTAGE - 3.3V operation; Increased field inversion voltage between adjacent MOSFETs, and reduced parasitic capacitance, with reduced additional field boron doping; without charge pump.
(Reissued from week 9418 to amend entry/ Reprinted in week 9422)
Dwg.6/8
Title Terms: NMOS; INTEGRATE; CIRCUIT; ELECTRIC; ISOLATE; ADJACENT; TRANSISTOR; FORWARD; BIAS; DIODE; VOLTAGE; DROP; GENERATE; BACK; BIAS; DIODE; CONNECT; GROUND; BODY; NMOS; TRANSISTOR; SURFACE
Derwent Class: U13
International Patent Class (Main): H01L-027/02; H01L-027/04

International Patent Class (Additional): H01L-021/76; H01L-021/822
File Segment: EPI

34/5/17 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008839518 **Image available**
WPI Acc No: 1991-343534/199147
XRPX Acc No: N93-102862
Facsimile appts. with electronic telephone directory - sequentially processes data from each communication device in socket to handle all data in card operated NoAbstract Dwg 3,5,6/14
Patent Assignee: CANON KK (CANO)
Inventor: SAKAMOTO T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3229564	A	19911011	JP 9023788	A	19900202	199147	B
US 5204758	A	19930420	US 91644443	A	19910122	199317	

Priority Applications (No Type Date): JP 9023788 A 19900202; JP 9016810 A 19900125; JP 9019735 A 19900130; JP 9020728 A 19900131; JP 9020729 A 19900131; JP 9020730 A 19900131; JP 9025490 A 19900205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5204758	A		30	H04N-001/40	

Abstract (Basic): JP 3229564 A

Insulating layer is formed on a semiconductor substrate. A polycrystal Si layer is formed on the insulating layer by CVD. The size of Si crystal particles forming the Si layer is adjusted so that the coefficient of the resistor value change of an electrical resistor device over temp. change may be zero.

USE/ADVANTAGE - Electrical resistor device is used in semiconductor devices, including ICs. The electrical resistor device requires no circuit compensating temp. change. The device has negative temp. characteristics, preventing thermal runaway. (4pp Dwg.No.2/4)

Title Terms: FACSIMILE; APPARATUS; ELECTRONIC; TELEPHONE; DIRECTORY; SEQUENCE; PROCESS; DATA; COMMUNICATE; DEVICE; SOCKET; HANDLE; DATA; CARD; OPERATE; NOABSTRACT
Derwent Class: T01; T04; W01; W02
International Patent Class (Main): H04N-001/40
File Segment: EPI

34/5/18 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008825563
WPI Acc No: 1991-329576/199145
XRPX Acc No: N93-102862
Facsimile equipment using data cards - has function for loading data memory cards and transferring data between cards NoAbstract Dwg 12/13
Patent Assignee: CANON KK (CANO)
Inventor: SAKAMOTO T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3220857	A	19910930	JP 9016810	A	19900125	199145	B
US 5204758	A	19930420	US 91644443	A	19910122	199317	

Priority Applications (No Type Date): JP 9016810 A 19900125; JP 9019735 A 19900130; JP 9020728 A 19900131; JP 9020729 A 19900131; JP 9020730 A

19900131; JP 9023788 A 19900202; JP 9025490 A 19900205
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 5204758 A 30 H04N-001/40

Abstract (Basic): JP 3220857 A
The silica sealing tube has double side wall and between the internal wall and external wall water can be flowed.
USE/ADVANTAGE - Used for annealing, e.g. II-VI cpd. semiconductor crystals, enabling quenching of the entire tube after annealing to ensure safety. (3pp Dwg.No.1,2/4)U
Title Terms: FACSIMILE; EQUIPMENT; DATA; CARD; FUNCTION; LOAD; DATA; MEMORY ; CARD; TRANSFER; DATA; CARD; NOABSTRACT
Derwent Class: T01; T04; W01; W02
International Patent Class (Main): H04N-001/40
File Segment: EPI

34/5/19 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

008493620 **Image available**
WPI Acc No: 1990-380620/199051
XRPX Acc No: N92-037735
Forming desired radiation pattern with array antenna - suppressing unwanted side-lobes by compensating for irregular density of antenna elements and matching null positions with Taylor pattern
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Number of Countries: 002 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 2276302 A 19901113 JP 8998032 A 19890418 199051 B
US 5081463 A 19920114 US 89457489 A 19891227 199206

Priority Applications (No Type Date): JP 8998032 A 19890418; JP 8993793 A 19890413

Abstract (Basic): JP 2276302 A
Semiconductor circuit bump is made by laminating selectively Pd, and Ni-alloy in sequence on a wiring metal of a semiconductor IC, to form external terminal on which Au and a metal having up to 350 deg.C m.pt. are laminated.
USE - For semiconductor circuit bump, forming uniformly a laminated height of low m.pt. metals e.g. solder, and preventing bonding faults. (4pp DWg.No.1/2)
Title Terms: FORMING; RADIATE; PATTERN; ARRAY; ANTENNA; SUPPRESS; UNWANTED; SIDE; LOBE; COMPENSATE; IRREGULAR; DENSITY; ANTENNA; ELEMENT; MATCH; NULL ; POSITION; TAYLOR; PATTERN
Derwent Class: W02; W06
International Patent Class (Additional): G01S-003/16; H01Q-003/26; H01Q-021/06
File Segment: EPI

34/5/20 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

008425583 **Image available**
WPI Acc No: 1990-312584/199042
XRPX Acc No: N90-239931
Telephone subset loudspeaker amplifier IC protection arrangement - has transducer to convert received speech and ringer signals into acoustic power, senses current to produce control signal

Patent Assignee: STANDARD TEL & CABLES LTD (STTE)
Inventor: SHAWFOX R C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
AU 9049305	A	19900830	AU 9049305	A	19900212	199042	B

Priority Applications (No Type Date): AU 892866 A 19890223; AU 9049305 A 19900212

Abstract (Basic): AU 9049305 A

The telephone subset incorporates an acoustic transducer for converting into acoustic power both received speech signals when the subset is in a first mode and AC ringer tone-call signals when the subset is in a second mode. The speech signals are amplified in the form of an integrated circuit whose output is coupled to the acoustic transducer. The ringer tone-call signals being generated in a ringer circuit whose output is coupled to the acoustic transducer in parallel with the output of the integrated circuit.

Excessive current is prevented from flowing in outputs of the integrated circuit when ringer tone-call signals are generated. The integrated circuit is caused to draw current via a forward biased **semiconductor** . The **current** is **sensed** through the **semiconductor** junction and thereupon produces a control signal. The control signal is applied to the integrated circuits disabling circuit to render the integrated circuit into a low current mode.

USE - For allowing speech to be received and transmitted without using handset.

Dwg.1/1

Title Terms: TELEPHONE; SUBSET; LOUDSPEAKER; AMPLIFY; IC; PROTECT; ARRANGE; TRANSDUCER; CONVERT; RECEIVE; SPEECH; RING; SIGNAL; ACOUSTIC; POWER; SENSE; CURRENT; PRODUCE; CONTROL; SIGNAL
Index Terms/Additional Words: HAND; FREE
Derwent Class: U24; W01
International Patent Class (Additional): H04M-001/60; H04M-019/02
File Segment: EPI